3 – 10GHz UWB Low Noise Amplifier

Preliminary Datasheet
VMMK-3803

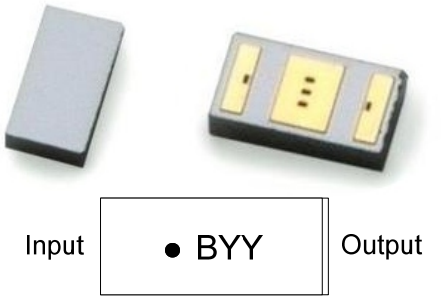
v.3.0 01/26/10 LN

Description

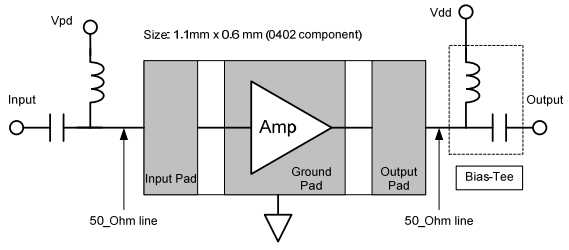
The VMMK-3803 is an easy-to-use, low noise and broad-band amplifier from 3-10GHz. It is housed in the Avago Technologies's industry-leading and revolutionary sub-miniature chip scale package. The VMMK-3803 features low noise, and good input, output match from 3-10GHz. The broad-band and low noise performance, coupled with an ultra compact package make this amplifier ideal for broad-band applications in the 3-10GHz band.

Avago's GaAsCap wafer scale leadless package is small and ultra thin yet can be handled and placed with standard 0402 pick and place assembly equipment.

WLP 0402 (1x0.5x0.25mm) Top, Bottom View



Note:
"B" = Device Code
"YY" = Year Code



Features

- **1 x 0.5 mm Surface Mount Package**
- **Ultrathin (0.25mm)**
- **Broadband Match to 50 ohm**
- **Frequency Range 3 to 10 GHz**
- **High Average Gain of 18dB**
- **Low Noise Figure**
- **Power-down capability through input**
- **Positive Supply**

Specifications (Vdd = 3.0V, Vpd=3.0V, Idd = 20mA)

- **Small-Signal Gain: 18 dB typ. at 6 GHz**
- **Noise Figure : 1.6 dB typ. at 6 GHz**
- **Output Intercept Point : +18 dBm typ at 6 GHz**

Applications

- **UWB LNA**

Attention:
Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A)
ESD Human Body Model (Class 1A)
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control

RoHS✓ EARTH FRIENDLY

Table 1. Absolute Maximum Ratings [1]

Sym	Parameters/Condition	Unit	Absolute Max
Vd	**Supply Voltage (RF Output)[2]**	**V**	**7V**
Vpd	**Power Down Voltage**	**V**	**3V**
Id	**Device Current [2]**	**mA**	**TBD**
$P_{in,\ max}$	**CW RF Input Power (RF Input) [3]**	**dBm**	**15**
P_{diss}	**Total Power Dissipation**	**mW**	**TBD**
Tch	**Max channel temperature**	**$_oC$**	**+150**
T_{STG}	**Storage Temperature**	**^oC**	**+150**
θjc	**Thermal Resistance [4]**	**$^oC/W$**	**90.6**

Notes
1. Operation of this device above any one of these parameters may cause permanent damage
2. Bias is assumed DC quiescent conditions
3. With the DC (typical bias) and RF applied to the device at board temperature Tb= 25^oC
4. Thermal resistance is measured from junction to board using IR method

DC and RF Specifications T_A= 25^{o}C, Freq=6GHz, Vd=3V, Vpd=3V I_{dd}=20mA, Z_{in}=Z_{out}=50Ω (unless otherwise specified)

Symbol	Parameters / Condition	Unit	Min	Typical	Max
Idd	**Supply Current**	**mA**	**14**	**20**	**22**
S11	**Input Return Loss**	**dB**		**15**	
S22	**Output Return Loss**	**dB**		**9**	
Ga	**Associated Gain**	**dB**	**16.5**	**18**	**19.5**
NF	**Noise Figure**	**dB**		**1.6**	**1.9**
OIP3	**Output 3rd Order Intercept Point**	**dBm**	**16**	**18**	

Notes:
1. Losses of the test system have been de-embedded from final data
2. Measured Data obtained from wafer-probing using a G-S, S-G pyramid probe
3. OIP3 test condition: F1=5.0GHz, F2=5.01GHz, Pin=-15dBm

VMMK-3803 Typical Performance

(T_A = 25°C, Vdd=3V, Vpd=3V Idd=20mA, Z_{in} = Z_{out} = 50 Ω unless noted)

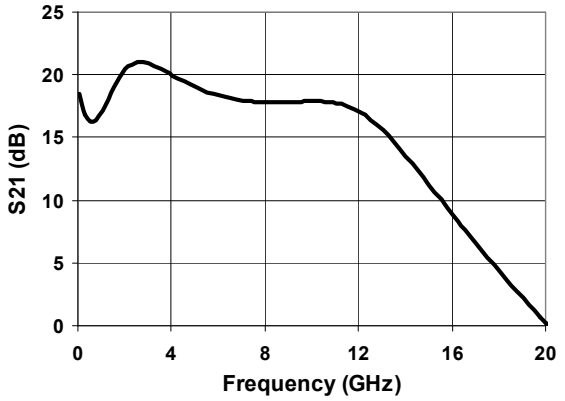


Figure 1. Small Signal Gain

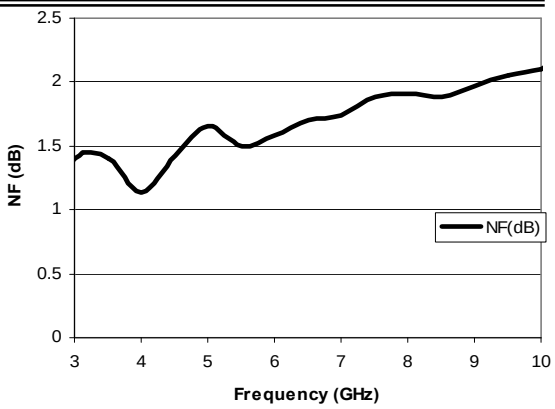


Figure 2. Noise Figure

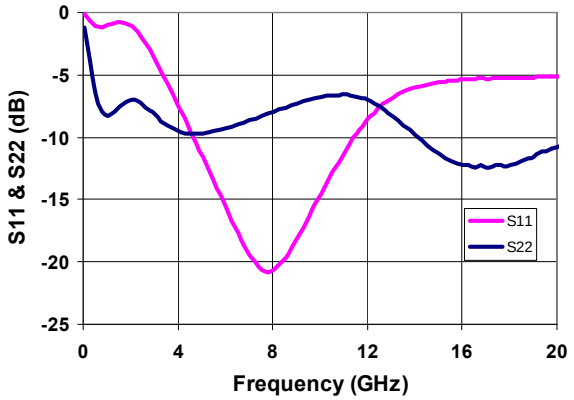


Figure 3. Input and Output Return Losses

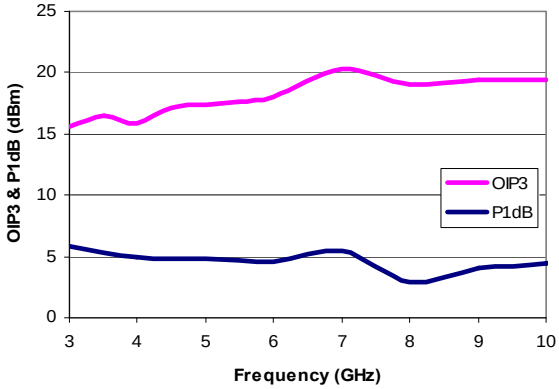


Figure 4. Output Power and IP3

Typical Scattering Parameters

T_A = 25°C, Vdd=3V, Vpd=3VV, I_{dq}=20mA, Z_{in} = Z_{out} = 50 Ω unless noted, Data obtained using 250um G-S-G PCB substrate & broadband bias tees, losses calibrated out to the package reference plane.

Freq	S11			S21			S12			S22		
GHz	dB	mag	Phase	dB	mag	phase	dB	mag	phase	dB	mag	Phase
0.1	-0.2	0.978	-5.384	18.2	8.085	154.205	-51.0	0.003	-7.365	-1.8	0.817	-15.061
0.2	-0.4	0.952	-10.417	17.5	7.480	135.332	-44.8	0.006	17.274	-2.8	0.727	-23.095
0.3	-0.7	0.927	-15.344	16.8	6.897	116.770	-41.4	0.009	40.121	-3.9	0.638	-30.841
0.4	-0.8	0.908	-18.308	16.6	6.723	103.871	-40.6	0.009	30.303	-4.9	0.571	-33.357
0.5	-1.0	0.889	-21.271	16.3	6.550	90.972	-39.9	0.010	20.485	-6.0	0.503	-35.872
0.6	-1.1	0.879	-24.186	16.3	6.504	80.413	-39.6	0.010	12.273	-6.8	0.457	-36.581
0.7	-1.1	0.877	-27.060	16.3	6.560	71.739	-39.6	0.011	5.354	-7.4	0.427	-35.834
0.8	-1.2	0.875	-29.960	16.4	6.627	63.168	-39.5	0.011	-1.493	-8.0	0.398	-35.070
0.9	-1.1	0.880	-33.298	16.7	6.854	56.301	-39.9	0.010	-7.148	-8.1	0.392	-34.001
1.0	-1.1	0.886	-36.636	17.0	7.082	49.433	-40.3	0.010	-12.804	-8.3	0.386	-32.932
2.0	-1.0	0.886	-80.559	20.3	10.408	-14.009	-60.8	0.001	11.269	-7.0	0.444	-50.063
3.0	-3.6	0.659	-126.591	20.9	11.098	-72.693	-39.3	0.011	59.971	-8.2	0.391	-77.995
4.0	-7.4	0.426	-162.388	20.0	9.977	-118.386	-35.2	0.017	30.510	-9.5	0.335	-94.239
5.0	-11.4	0.270	169.415	19.0	8.936	-155.852	-33.3	0.022	9.641	-9.7	0.327	-107.669
6.0	-15.5	0.169	147.432	18.3	8.264	170.470	-32.2	0.025	-7.870	-9.3	0.344	-123.730
7.0	-19.3	0.108	135.794	17.9	7.888	138.334	-31.2	0.028	-24.607	-8.7	0.368	-142.327
8.0	-20.7	0.093	136.431	17.8	7.766	106.217	-30.3	0.030	-42.322	-8.0	0.399	-163.598
9.0	-18.2	0.123	127.687	17.8	7.782	72.983	-29.6	0.033	-61.665	-7.3	0.431	172.340
10.0	-14.6	0.185	101.568	17.9	7.842	37.775	-29.2	0.035	-83.593	-6.8	0.458	145.187
11.0	-11.3	0.272	65.774	17.8	7.723	-0.219	-29.2	0.035	-109.633	-6.6	0.468	113.694
12.0	-8.6	0.370	26.363	17.1	7.153	-40.441	-30.3	0.031	-138.504	-7.0	0.446	78.746
13.0	-6.9	0.452	-12.657	15.7	6.063	-80.486	-32.5	0.024	-168.275	-8.2	0.389	41.515
14.0	-6.0	0.501	-47.580	13.6	4.795	-117.521	-36.3	0.015	160.972	-9.8	0.324	5.404
15.0	-5.6	0.527	-77.624	11.3	3.673	-150.759	-41.0	0.009	130.062	-11.3	0.271	-29.280
16.0	-5.4	0.538	-103.264	8.9	2.791	179.175	-47.0	0.004	83.461	-12.2	0.245	-62.209
17.0	-5.3	0.544	-125.149	6.6	2.139	151.736	-47.0	0.004	6.128	-12.4	0.240	-89.832
18.0	-5.2	0.547	-144.783	4.4	1.660	125.773	-43.4	0.007	-34.264	-12.2	0.245	-114.837
19.0	-5.2	0.550	-162.106	2.3	1.299	101.137	-40.7	0.009	-57.127	-11.6	0.264	-136.812
20.0	-5.2	0.553	-177.914	0.3	1.030	77.411	-39.0	0.011	-74.601	-10.8	0.287	-155.021

Typical Scattering Parameters

T_A = 25°C, Vdd=3V, Vpd=0V, I_{dq}=0.04uA, Z_{in} = Z_{out} = 50 Ω unless noted, Data obtained using 250um G-S-G PCB substrate & broadband bias tees, losses calibrated out to the package reference plane.

Freq	S11			S21			S12			S22		
GHz	dB	mag	Phase	dB	mag	phase	dB	mag	phase	dB	mag	Phase
0.1	-0.1	0.991	-2.346	-46.7	0.005	5.910	-48.2	0.004	29.207	0.0	0.998	-3.186
0.2	-0.1	0.992	-4.444	-47.0	0.004	23.229	-47.7	0.004	34.542	-0.1	0.992	-6.044
0.3	-0.1	0.992	-6.543	-47.3	0.004	39.571	-47.3	0.004	39.548	-0.1	0.987	-8.893
0.4	-0.1	0.991	-8.644	-46.4	0.005	38.121	-46.5	0.005	38.580	-0.2	0.976	-11.569
0.5	-0.1	0.990	-10.745	-45.7	0.005	36.671	-45.8	0.005	37.611	-0.3	0.965	-14.246
0.6	-0.1	0.989	-12.842	-45.2	0.005	35.799	-45.3	0.005	37.028	-0.4	0.952	-16.784
0.7	-0.1	0.987	-14.934	-45.1	0.006	35.392	-44.9	0.006	36.756	-0.6	0.938	-19.210
0.8	-0.1	0.985	-17.027	-44.9	0.006	34.982	-44.6	0.006	36.428	-0.7	0.924	-21.619
0.9	-0.1	0.985	-19.120	-44.9	0.006	34.515	-44.6	0.006	35.183	-0.8	0.910	-23.747
1.0	-0.1	0.984	-21.213	-45.0	0.006	34.048	-44.7	0.006	33.938	-1.0	0.895	-25.875
2.0	-0.3	0.970	-42.331	-39.8	0.010	120.508	-39.8	0.010	122.630	-2.2	0.774	-42.725
3.0	-0.8	0.914	-63.601	-24.3	0.061	89.002	-24.5	0.060	89.317	-3.0	0.712	-53.610
4.0	-1.1	0.884	-79.448	-20.3	0.097	20.056	-20.3	0.097	20.655	-2.5	0.752	-67.391
5.0	-0.8	0.910	-98.940	-21.0	0.089	-18.723	-21.0	0.089	-18.410	-2.5	0.746	-84.492
6.0	-0.8	0.914	-119.961	-21.5	0.084	-43.286	-21.5	0.084	-42.948	-2.7	0.734	-100.441
7.0	-0.8	0.910	-141.364	-21.6	0.084	-63.673	-21.6	0.083	-63.371	-2.8	0.725	-115.944
8.0	-0.9	0.901	-163.177	-21.5	0.084	-82.917	-21.5	0.084	-82.511	-2.9	0.719	-131.436
9.0	-1.0	0.888	174.555	-21.3	0.086	-102.061	-21.3	0.086	-101.407	-2.9	0.715	-147.131
10.0	-1.2	0.875	151.629	-21.0	0.089	-121.166	-21.0	0.089	-120.858	-2.9	0.712	-162.725
11.0	-1.3	0.859	127.713	-20.5	0.094	-141.409	-20.5	0.094	-140.994	-3.0	0.705	-178.820
12.0	-1.5	0.843	102.811	-19.8	0.102	-162.634	-19.9	0.101	-162.075	-3.1	0.699	164.769
13.0	-1.7	0.822	76.523	-19.0	0.112	174.561	-19.0	0.113	175.218	-3.3	0.683	147.565
14.0	-1.9	0.800	48.949	-17.8	0.129	148.993	-17.9	0.128	149.649	-3.7	0.652	129.111
15.0	-2.2	0.774	20.169	-16.3	0.153	120.425	-16.3	0.153	120.815	-4.6	0.590	109.101
16.0	-2.6	0.742	-9.048	-14.4	0.190	85.199	-14.5	0.189	85.681	-6.9	0.453	87.865
17.0	-2.9	0.712	-36.492	-12.9	0.227	39.755	-12.9	0.226	40.733	-13.0	0.223	87.718
18.0	-2.9	0.719	-61.917	-13.3	0.216	-13.451	-13.2	0.218	-11.999	-8.5	0.378	128.407
19.0	-2.4	0.755	-88.437	-15.8	0.162	-59.425	-15.7	0.165	-58.395	-3.9	0.635	102.134
20.0	-2.2	0.780	-114.300	-18.8	0.114	-95.177	-18.7	0.116	-94.380	-2.6	0.737	72.260

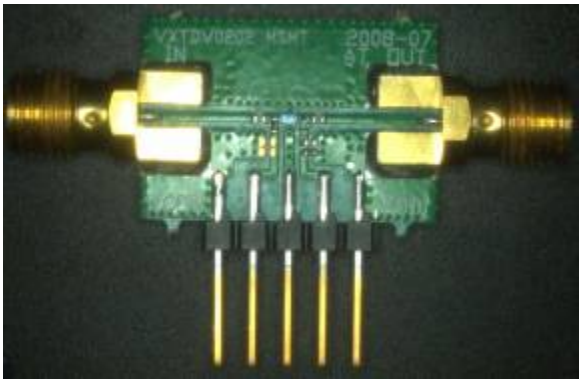


Figure 1. Evaluation/Test Board (available to qualified customers upon request)

Biasing and Operation

The VMMK-3803 is biased with a positive supply connected to the output pin Vd through an external user supplied bias decoupling network. Typical bias is 3V at 20 mA. The “on” state also requires that the input port of the VMMK-3803 also be biased at 3V for normal gain operation. 0V on the input puts the VMMK-3803 in the “off” state.

An example of simple user supplied bias tees is shown in Figure 1. The output bias decoupling network feeding Vdd consists of a shunt 6.8 nH inductor. At the input, a 10K ohm resistor is needed to feed the power-down control voltage. The input and output dc blocking capacitors are each 100 pF. The “on” and “off” S Parameters shown in the preceding tables reflect the operation of the circuit shown in Figure 1.

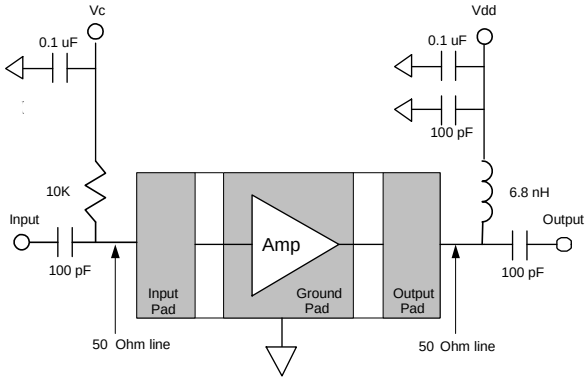


Figure 2. Biasing the VMMK-3803

A layout of a typical demo board is shown in Figure 3.

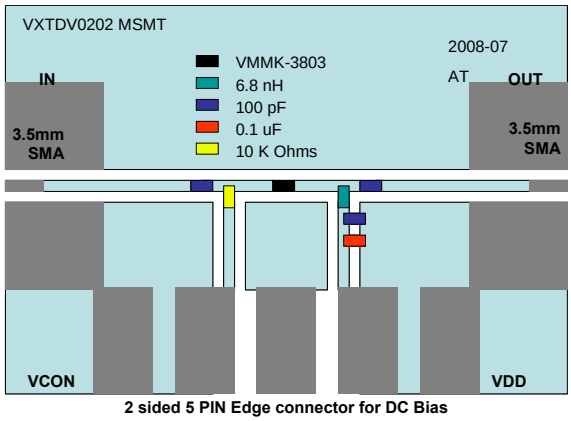


Figure 3. VMMK-3803 Demo board layout

The input and output bias decoupling network can be easily constructed using small surface mount components. The value of the shunt inductors can have a major effect on both low and high frequency operation. The demo board uses small value inductors that have self resonant frequencies higher than the maximum desired frequency of operation. If the self-resonant frequency of the inductor is too close to the operating band, the value of the inductor will need to be adjusted so that the self-resonant frequency is significantly higher than the highest frequency of operation.

Typically a passive component company like Murata does not specify S parameters at frequencies higher than 5 or 6 GHz for larger values of inductance making it difficult to properly simulate amplifier performance at higher frequencies. It has been observed that the Murata LQW15AN series of 0402 inductors actually works quite well above their normally specified frequency.

The parallel combination of the 100pF and 0.1uF bypass capacitors provide a low impedance in the band of operation and at lower frequencies and should be placed as close as possible to the inductor. The low frequency bypass provides good rejection of power supply noise and also provides a low impedance termination for third order low frequency mixing products that will be

generated when multiple in-band signals are injected into any amplifier.

S Parameter Measurements

The S parameters are measured on a .016 inch thick RO4003 printed circuit test board, using G-S-G (ground signal ground) probes. Coplanar waveguide is used to provide a smooth transition from the probes to the device under test. The presence of the ground plane on top of the test board results in excellent grounding at the device under test. TRL (Thru – Reflect – Line) calibration is used to correct for the effects of the test board, resulting in accurate device S-parameters.

Outline Drawing

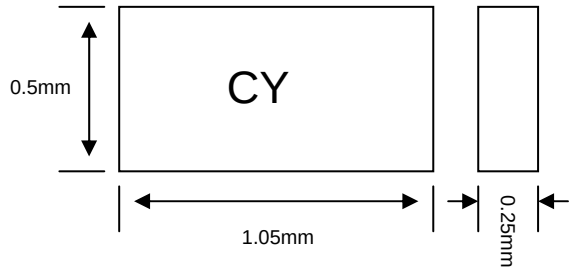


Figure 4. Top and Side View

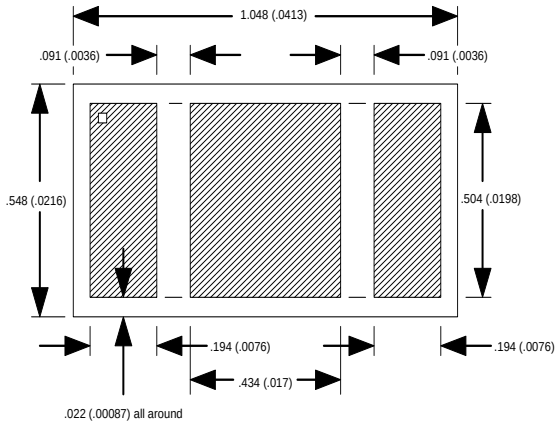


Figure 5. Bottom View

NOTES:

1. ● indicates pin 1
2. Dimensions are in millimeters
3. Pad Material is minimum 5.0 um thick Au/Ni/Au

Suggested PCB Material and Land Pattern

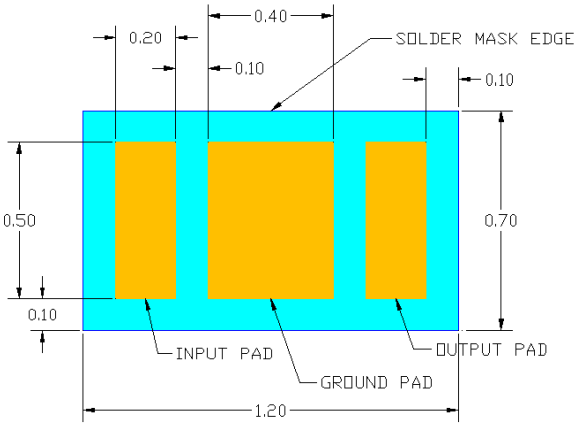


Figure 6. Recommended PCB land pattern

NOTES:

1. 0.010" Rogers RO4350

Recommended SMT Attachment

The VMMK Packaged Devices are compatible with high volume surface mount PCB assembly processes.

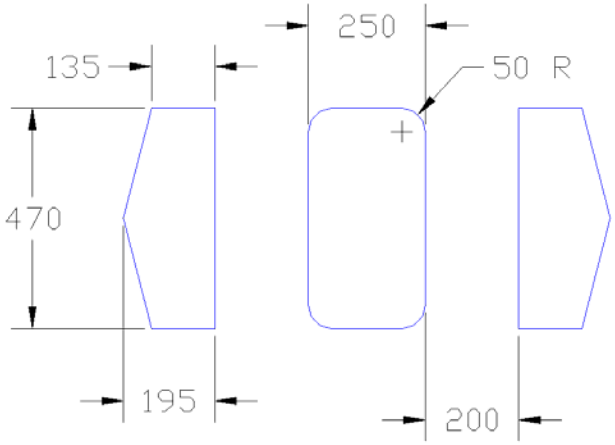


Figure 7. Suggested stencil pattern.

Notes:

1. Dimensions in microns
2. Stencil thickness 100 microns
3. Stencil type: laser cut.

Manual Assembly for Prototypes

1. Follow ESD precautions while handling packages.
2. Handling should be along the edges with tweezers or from topside if using a vacuum collet.
3. Recommended attachment is solder paste. Please see recommended solder reflow profile. Conductive epoxy is not recommended. Hand soldering is not recommended.
4. Apply solder paste using either a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance. ***Excessive solder will degrade RF performance.***
5. Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temp to avoid damage due to thermal shock.

6. Packages have been qualified to withstand a peak temperature of 280°C for 15 sec. Verify that the profile will not expose device beyond these limits.
7. Clean off flux per vendor's recommendations.
8. Clean the module with Acetone. Rinse with alcohol. Allow the module to dry before testing.

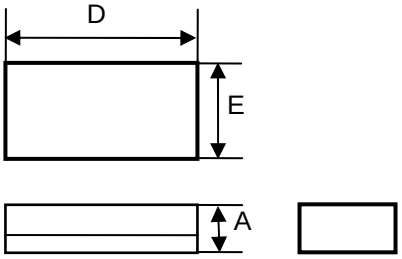
Note: These devices are ESD sensitive. The following precautions are strongly recommended. Ensure that an ESD approved carrier is used when die are transported from one destination to another. Personal grounding is to be worn at all times when handling these devices. For more detail, refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control

ESD Machine Model (Class A)
ESD Human Body Model (Class A)

Ordering Information

Part Number	Devices Per Container	Container
VMMK-3803-BLKG	100	Antistatic Bag
VMMK-3803-TR1G	5000	7" Reel

Package Dimension Outline

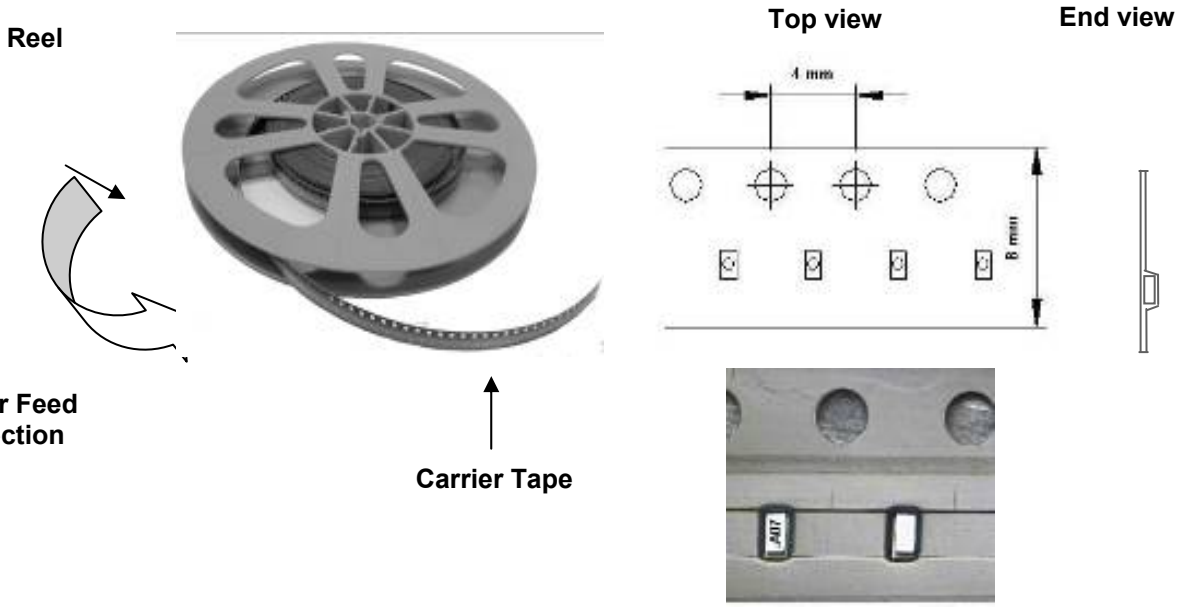


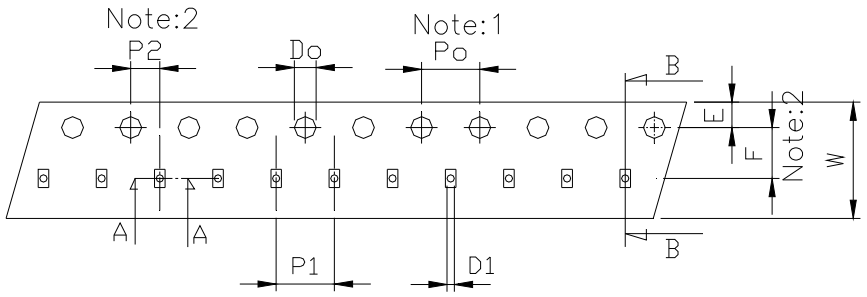
Dimensions

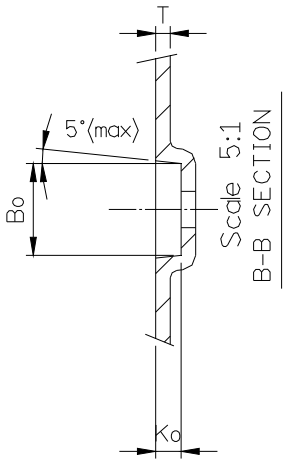
Symbol	Min (mm)	Max (mm)
E	0.500	0.566
D	1.004	1.066
A	0.235	0.265

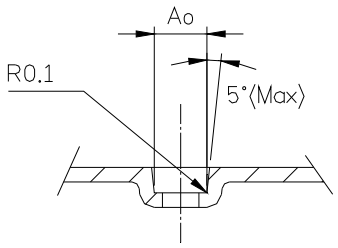
Note:
All dimensions are in mm

Device Orientation









Scale 5:1
A–A SECTION

Ao= 0.73± 0.05 mm

Bo= 1.26± 0.05 mm

Ko= $0.35^{+0.05}_{+0}$ mm

Unit: mm

Symbol	Spec.
K1	–
Po	4.0± 0.10
P1	4.0± 0.10
P2	2.0± 0.05
Do	1.55± 0.05
D1	0.5± 0.05
E	1.75± 0.10
F	3.50± 0.05
10Po	40.0± 0.10
W	8.0± 0.20
T	0.20± 0.02

Notice:

1. 10 Sprocket hole pitch cumulative tolerance is ±0.1mm
2. Pocket position relative to sprocket hole measured as true position of pocket not pocket hole.
3. Ao & Bo measured on a place 0.3mm above the bottom of the pocket to top surface of the carrier.
4. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Carrier camber shall be not than 1mm per 100mm through a length of 250mm.

For product information and a complete list of Avago contacts and distributors, please go to our Website:
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Data subject to change.