

Avago introduces 18 GHz and 26.5 GHz low-noise E-pHEMT in 0402 Compatible Packages Produced by Advanced Wafer-scale Packaging Technology



White Paper

Introduction

Smaller, lower cost components are crucial to the development of today's higher-performance, smaller and increasingly price-competitive mobile devices. Since the introduction of chip scale packages (CSPs) they have become a major trend in active device packaging. Chip scale packaging combines the size and performance advantage of bare die assembly and the reliability of encapsulated devices, while permitting automated assembly processes and low production costs.

Chip Scale Packages

According to the IPC/JEDEC J-STD-012 definition, a chip scale package is a single-die, surface-mountable package with an area of no more than 1.2 times the area of the original die. This definition is somewhat fluid, since, for example, there have been cases of original die being shrunk due to process changes and improvements with customers requiring that the resulting CSP be unchanged. There are also multi-layer CSPs that incorporate several stacked active devices. There is no overall definition of how a chip-scale package is to be constructed, so any package that meets the surface-mounting and dimensional requirements of the definition is a CSP.

Some CSP implementations are peripheral arrays, in many ways comparable to plastic leaded chip carriers (PLCCs); others feature either pads or solder bumps (ball-grid arrays) over the bottom of the component. In many packages the actual chip is bonded to the top of an interposer – a ceramic substrate – with electrical connections made either by wire bonding or via bumps on a flip chip. In this case, the actual pins, pads or bumps to interface with a printed-circuit board are on the bottom of the interposer substrate.

Wafer-scale packaging (WSP), also known as wafer-level packaging (WLP) or wafer-level chip scale packaging (WLCSP), essentially consists of extending the wafer fabrication processes to include packaging. This contrasts with the common approach of dicing a wafer into individual die, which are each packaged separately. WSP represents an optimized form of chip-scale packaging technology, since the resulting package is practically of the same size as the die. Wafer scale packaging paves the way for integration of wafer fab, packaging, test, and burn-in at wafer level, for the ultimate streamlining of the manufacturing process start to shipment. It also maximizes the footprint available to the device while minimizing the overall package size. The die or substrate itself becomes an integral part of the package rather than requiring the die or device to be encapsulated within a secondary level package. WSP can be referred to as "zero-level packaging," to distinguish it from first-level packaging, which connects the die to a lead frame or separate package.

Avago Technologies developed a bonded-wafer-to-wafer package, for its FBAR (film bulk acoustic resonator) MEMS filters and duplexers, with the first products introduced in 2004. Now Avago has developed an innovative microwave/millimeter-wave-capable gallium arsenide (GaAs) wafer scale package, the WaferCap chip scale package, that can provide surface-mount (SMT) devices operating at, potentially, up to 100 GHz at a very low package cost.

WaferCap chip scale packaging consists of a device wafer and a cap wafer joined with a polymer gasket seal. The seal gasket encloses the perimeter of the die. The result is an air-cavity wafer-scale package, which differentiates it from most other WSP technologies currently in use. The air cavity provides the necessary clearance between the active device and the metal and dielectric of the cap wafer to permit high-frequency operation and provides mechanical protection for the device during use.

On completion of the base integrated circuit wafer, the cap wafer is aligned and sealed to the device wafer. When the completed devices are sawed apart, the combination of the gasket and cap wafer provides an air cavity, structural support and protection for the device wafer. Since the device wafer contains thousands of individual devices, when the two wafers are sawn between the gaskets, the result is thousands of individual parts. All inputs and outputs (I/Os) are routed through via-holes to the backside of the device wafer eliminating performance limiting wire bonds.

A cross section of the wafer scale package is shown in Figure 1. The base GaAs wafer is fabricated using standard processes. The backside vias and I/O pads serve as the lead-frame of the package. The backside metal is thick enough to ensure adequate coverage in the bottom of the vias without inhibiting the use of standard solder paste in assembly.

The initial Avago WaferCap package is designed with a 0402 (1 mm x 0.5 mm)-compatible dimension, a 0.25 mm height, and full surface mount capability. Because all I/Os are routed to the backside of the device wafer through vias, the RF transitions suffer almost no signal loss and minimal parasitics. This is a significant improvement over conventional plastic packages where bond wires contribute substantial parasitics that degrade the performance.

The 0402 package is widely used, with components ranging from chip capacitors and inductors to LEDs, fuses, and Schottky and zener diodes. This means that the Avago wafer cap package is fully compatible with existing low cost, high volume assembly and test equipment. Figure 2 shows a 6-inch capped GaAs wafer, the die sawing process, as well as a bottom view of the 0402 package.

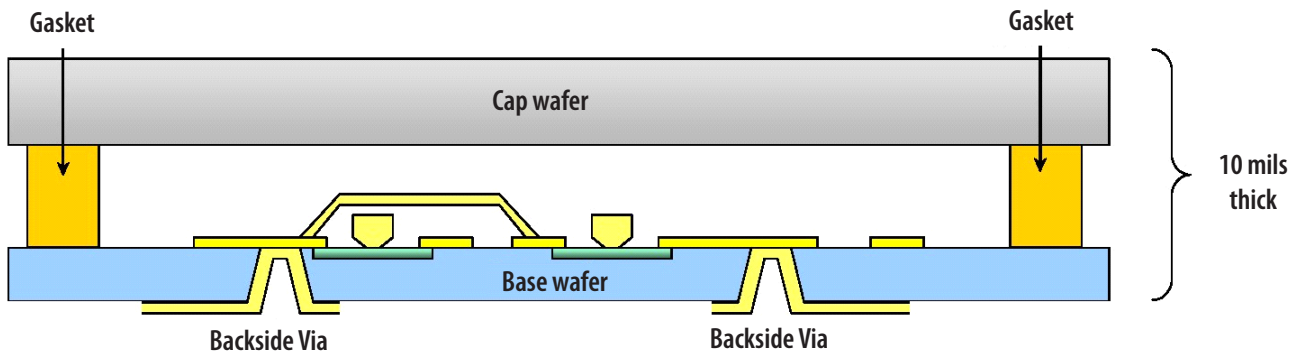


Figure 1. Cross-section view of Avago's WaferCap chip scale package. The cap wafer provides the lid, while the base wafer incorporates the active device with outside I/O connections made through hermetic vias. The gasket is a patterned polymer.

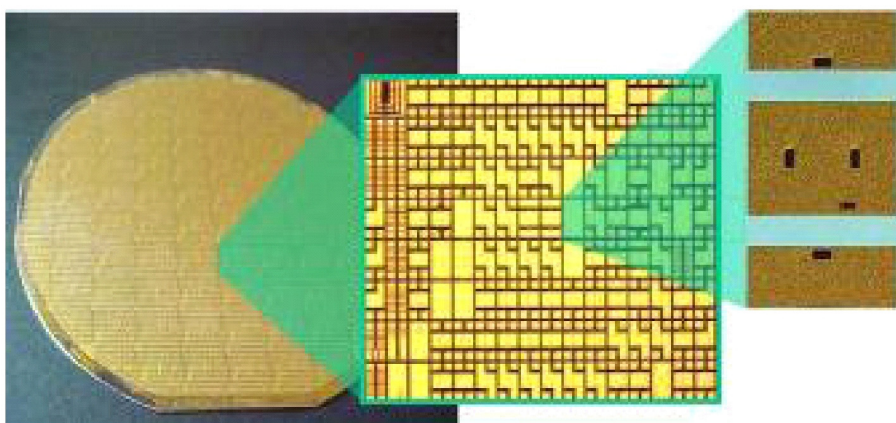


Figure 2. The basic wafer cap chip scale package fabrication process. Left shows an assembled six-inch cap and base wafer. Center shows the sawing process. Right is a bottom view of a resulting 0402 chip-scale packaged device.

The pad size and separation are adequate to ensure that no special package footprint concessions need to be made by customers. Lead free solder paste is the recommended adhesive, as it will help the parts to self-align on a PC board.

In the initial WaferCap chip scale products, Avago is using its industry leading enhancement-mode pseudomorphic high electron mobility transistor (E-pHEMT) technology. The result is transistors that feature high dynamic range, ultra-low noise, high gain and operation from a single positive DC supply

The use of 0.25- μm gate length devices combines an ultra low noise figure with substantial associated gain. With a flat transconductance over bias and frequency the transistors provide excellent linearity. These devices are easy to use, since they require only a single positive DC voltage for bias. They feature low matching coefficients for simple impedance matching to 50 Ω systems.

Two of the new devices are the VMMK-1218, DC to 18 GHz, and VMMK-1225 DC to 26.5 GHz low-noise E-pHEMTs. Both devices are available on tape-and-reel for pick and place assembly equipment.

The Avago VMMK-1218 is an E-pHEMT device with a 400- μm gate width. Typical performance (3.0V, 20 mA typ. bias @ 10 GHz) includes < 1.0 dB noise figure, 15 dB available gain, +30 dBm output 3rd order intercept point and +15 dBm output.

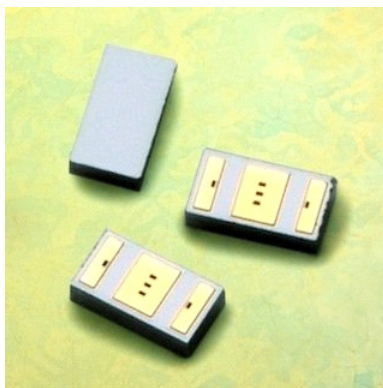


Figure 3. Top and bottom views of the Avago WaferCap chip scale E-pHEMT devices in 0402-compatible packages.

The Avago VMMK-1225 is an E-pHEMT device with 200- μm gate width. Typical performance (2.0V, 20 mA typ. bias @ 12 GHz) includes < 1.0 dB noise figure, 12 dB available gain, +31 dBm output 3rd order intercept point and +10 dBm output power.

Figure 3 shows a top view of the VMMK-1218, and bottom views of both devices. Figure 4 shows a VMMK-1225 mounted on a demonstration board.

Both devices are suitable for a wide range of applications including:

- Low noise and driver amplifier for cellular/PCS and WCDMA base stations;
- 2.4 GHz, 3.5 GHz, 5-6 GHz WLAN and WiMax notebook computers, access points and other mobile wireless equipment;
- 10 to 13 GHz direct broadcast satellite (DBS) receivers;
- 13 to 18 GHz very small aperture terminal (VSAT) and other satellite communications equipment;
- IEEE 802.16 and IEEE 802.20 broadband wireless access systems;
- Wireless local loop (WLL) and multi-channel multi-point distribution system (MMDS) transceivers;
- Military radar, radio and ECM systems.

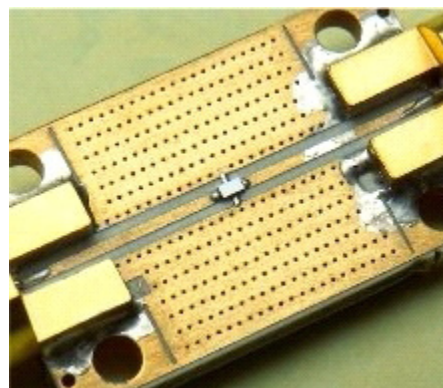


Figure 4. Avago WaferCap VMMK-1225 low-noise E-pHEMT mounted on a demonstration board.

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

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