

VMMK-2103

0.5 to 6 GHz Bypass E-PHEMT LNA in Wafer Scale Package

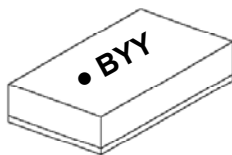


Preliminary Datasheet

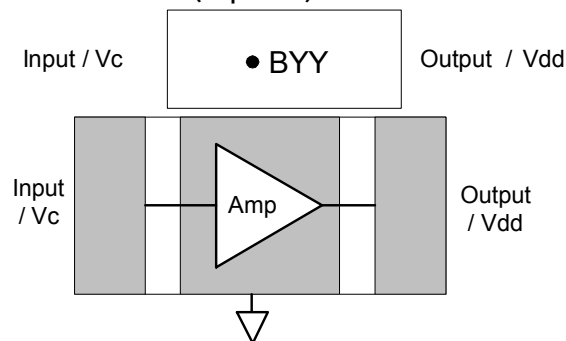
Description

Avago's VMMK-2103 is an easy-to-use GaAs MMIC bypass LNA that offers good noise figure and flat gain from 0.5 to 6 GHz in a miniaturized wafer-scale SMT package. The bias circuit is fitted with a power down feature which is accessed from the input port by way of an external resistor. This device contains an integrated bypass switch which engages when the amplifier is in shut down mode, resulting in an improvement in the input compression point while consuming minimal current. The input and output are matched to 50 Ω (better than 2:1 SWR) across the entire bandwidth; no external matching is needed. This amplifier is fabricated with enhancement E-pHEMT technology and industry leading revolutionary wafer scale package. The WSP leadless package is small and ultra thin yet can be handled and placed with standard 0402 pick and place assembly.

WaferCap™ 0402, 1mm x 0.5mm x 0.25 mm



Pin Connections (Top View)



Note:
"B" = Device Code
"YY" = Year Code

Features

- 1 x 0.5 mm Surface Mount Package
- Low height (0.25mm)
- Bypass function
- 5V Supply
- Tape and Reel packaging option available

Specifications (at 3GHz, Vd=Vc=5V, 24mA Typ.)

- 1.7dB noise figure
- 14dB available gain
- 2.4dB loss in Bypass State (Vc=0V)
- 22dBm output 3rd order intercept
- 14dBm output P1dB

Applications

- Low Noise and Driver for Cellular/PCS and WCDMA Base Stations
- 2.4 GHz, 3.5GHz, 5-6GHz WLAN and WiMax notebook computer, access point and mobile wireless applications
- 802.16 & 802.20 BWA systems
- WLL and MMDS Transceivers
- Military Radar, radio and ECM systems



Attention:
Observe precautions for handling electrostatic sensitive devices.

ESD Machine Model (Class A)
ESD Human Body Model (Class 1A)
Refer to Avago Application Note A004R:
Electrostatic Discharge Damage and Control

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Preliminary Datasheet

Table 1. Absolute Maximum Ratings

Sym	Parameters/Condition	Unit	Absolute Max
Vd	Supply Voltage (RF Output) ^[2]	V	8
Vc	Bypass Control Voltage	V	5.5
Id	Device Current ^[2]	mA	50 mA
P _{in, max}	CW RF Input Power (RF Input) ^[3]	dBm	18 dBm
P _{diss}	Total Power Dissipation	mW	300 mW
T _{ch}	Max channel temperature	°C	+150
T _{STG}	Storage Temperature	°C	+150
Θ _{jc}	Thermal Resistance ^[4]	°C/W	110

Notes

1. Operation of this device above any one of these parameters can cause permanent damage
2. Bias is assumed DC quiescent conditions
3. With the DC (typical bias) and RF applied to the device at board temperature T_b = 25°C
4. Thermal resistance is measured from junction to board using IR method

Table 2. DC and RF Specifications

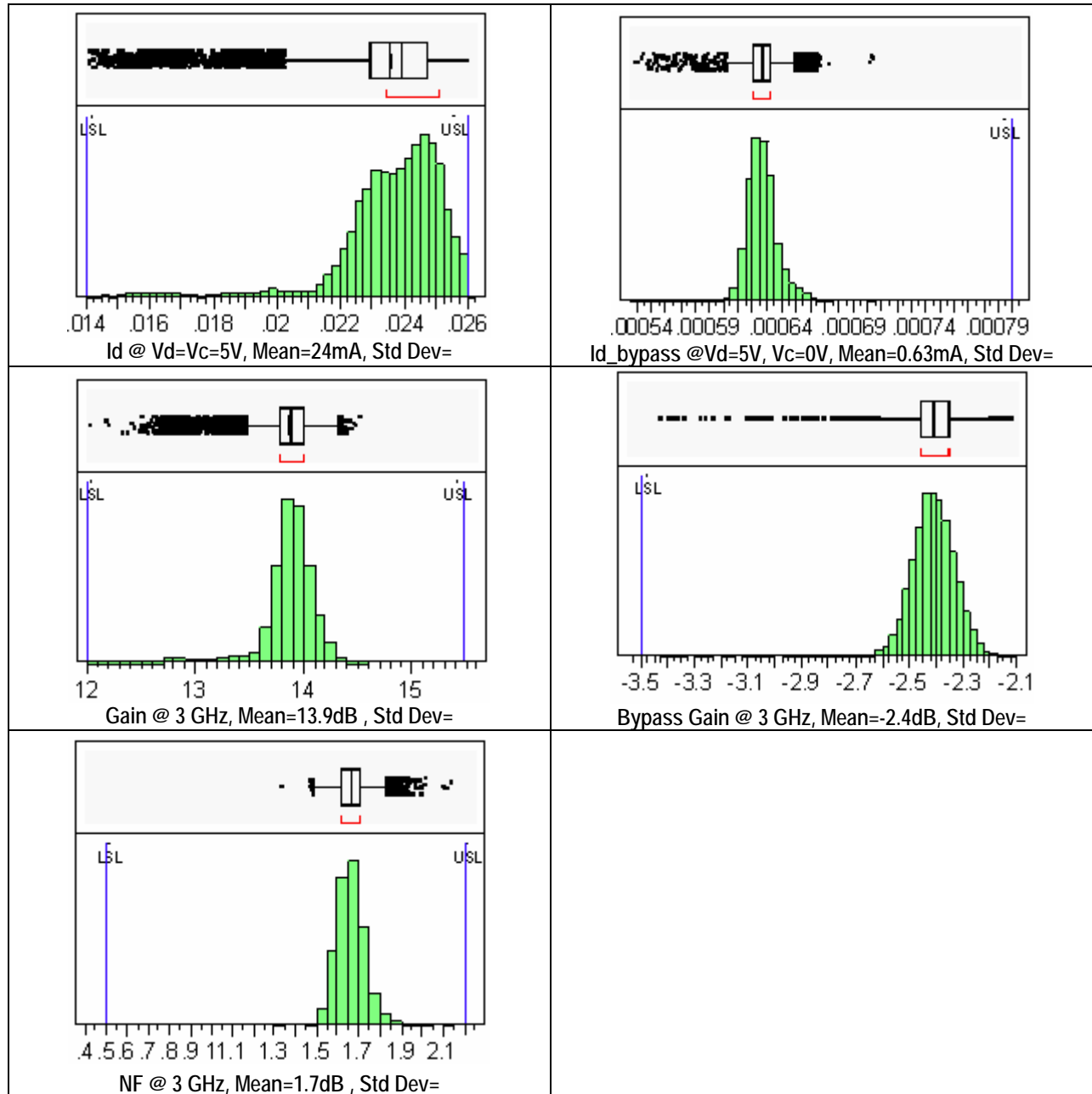
T_A = 25°C, Frequency = 3 GHz, Vd = 5V, Vc = 5V, I_d = 24mA, Z_{in} = Z_{out} = 50Ω (unless otherwise specified)

Sym	Parameters/Condition	Unit	Minimum	Typ.	Maximum
Id	Device Current	mA		24	
Id_leakage	Current in Bypass Mode	mA		0.6	
NF ^[1]	Noise Figure	dB	-	1.7	
Ga ^[1]	Associated Gain	dB	12	13.9	16
Ga_Bypass ^[1]	Associated Gain in Bypass Mode	dB	-3.5	-2.4	
IIP3_Gain ^[2,3]	Input IP3 in Gain Mode	dBm		8	-
IIP3_Bypass ^[2,4]	Input IP3 in Bypass Mode	dBm		21	
IP1dB_Gain ^[2]	Input Power at 1dB Gain Compression in Gain Mode	dBm		0	
IP1dB_Bypass ^[2]	Input P-1dB in Bypass Mode			17	
IRL ^[2]	Input Return Loss	dB	-	-10	-
ORL ^[2]	Output Return Loss	dB	-	-9	-

Notes:

1. Measure Data obtained using 300um G-S production wafer probe
2. Measure Data obtained using 300um G-S-G PCB substrate probe
3. IIP3 test condition: F1=6.0GHz, F2=6.01GHz, Pin=-10dBm in Gain State
4. IIP3 test condition: F1=6.0GHz, F2=6.01GHz, Pin=0dBm in Bypass State

Product Consistency Distribution Charts at 3.0 GHz, Vd = 5 V, Vc = 5V



Note: Distribution data based on 500 part sample size from 3 lots during initial characterization. Measurements were obtained using 300um G-S production wafer probe.

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VMMK-2103 Typical Performance [1], [2], [3]

($T_A = 25^\circ\text{C}$, $Z_{in} = Z_{out} = 50 \Omega$ unless noted)

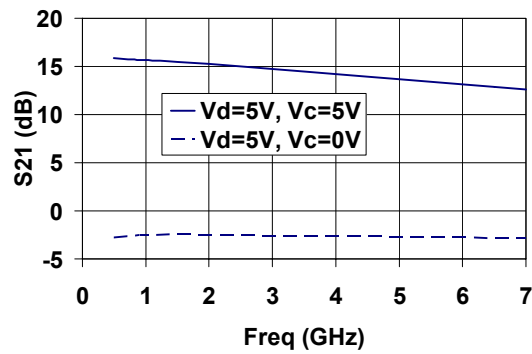


Figure 1. Small-signal Gain

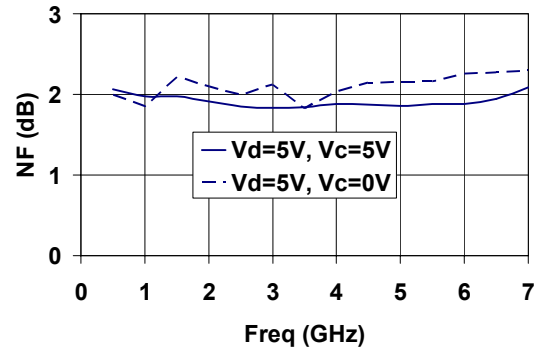


Figure 2. Noise Figure

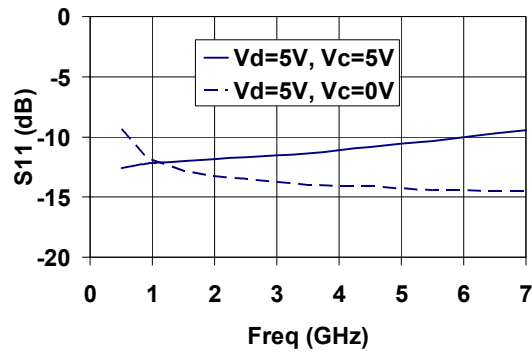


Figure 3. Input Return Loss

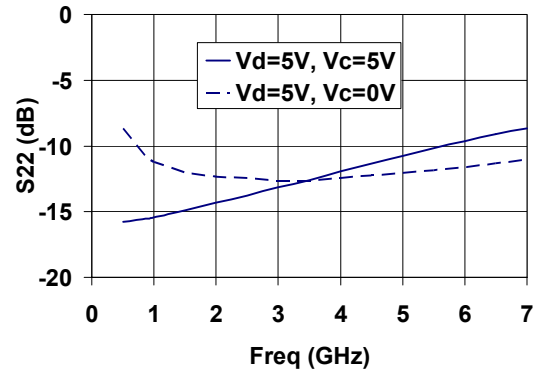


Figure 4. Output Return Loss

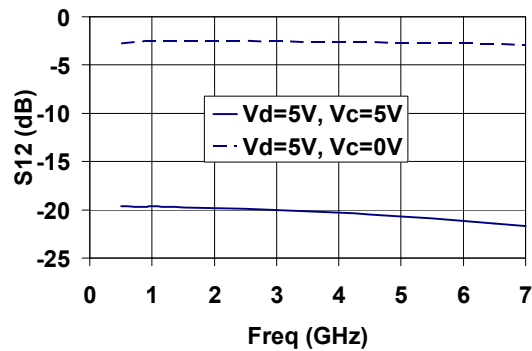


Figure 5. Isolation

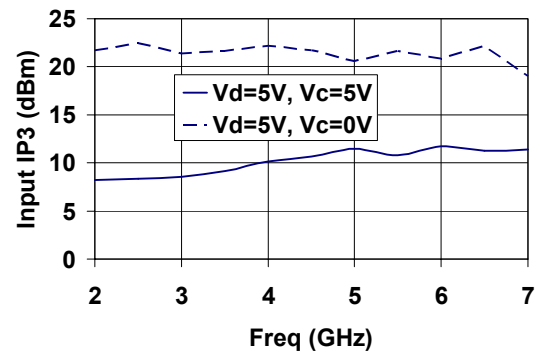


Figure 6. Input Third Order Intercept Point

Note:

- [1] Data are taken on a G-S-G substrate probe fully de-embedded
- [2] Noise Figure is measured on a G-S-G substrate probe in 50-Ohm environment
- [3] Input IP3 data for bypass state ($V_c=0V$) taken at $P_{in}=0dBm$; for Gain State, $P_{in}=-20dBm$

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VMMK-2103 Typical Performance (cont)

($T_A = 25^\circ\text{C}$, $Z_{in} = Z_{out} = 50 \Omega$ unless noted)

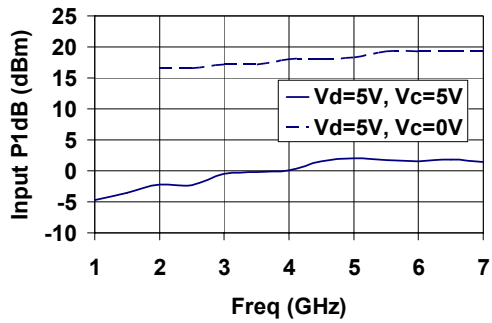


Figure 7. Input Power at 1dB Gain Compression

	Vdd=5V Vc=5V	Vdd=5V Vcc=0V	Vdd=3V Vc=3V	Vdd=3V Vc=0V
I _{dd}	24mA	0.6mA	10mA	0.4mA

Figure 8. Total Current

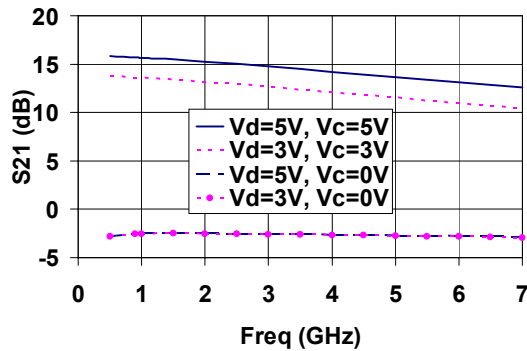


Figure 9. Gain Over Vdd

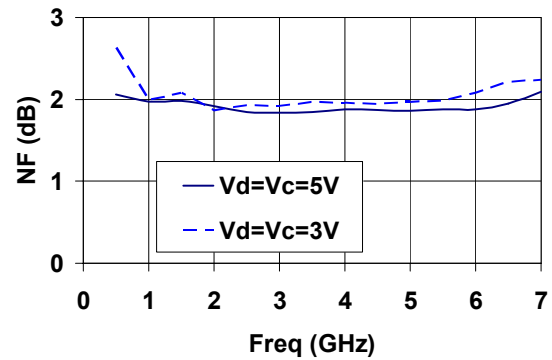


Figure 10 Noise Figure over Vdd

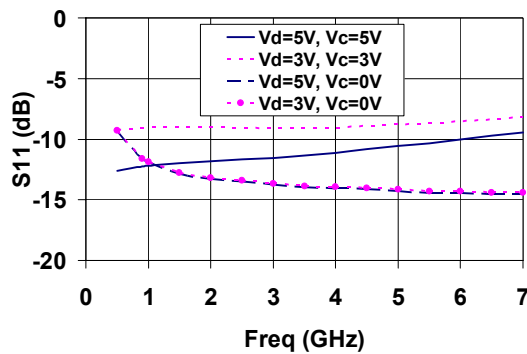


Figure 11. Input Return Loss over Vdd

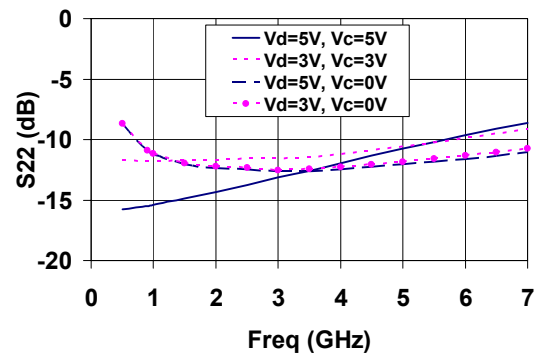


Figure 12. Output Return Loss Over Vdd

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VMMK-2103 Typical Performance (cont)

($T_A = 25^\circ\text{C}$, $Z_{in} = Z_{out} = 50\ \Omega$ unless noted)

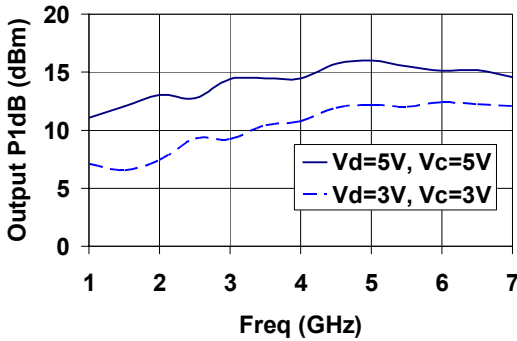


Figure 13. Output P1dB over Vdd in Gain Mode

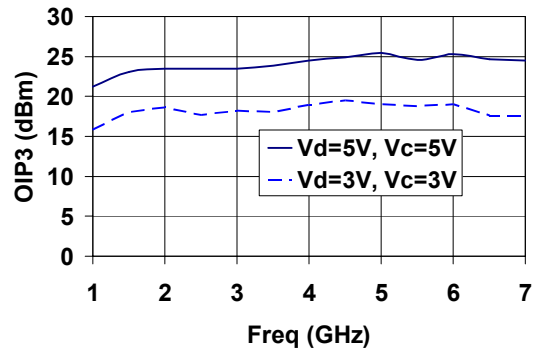


Figure 14. Output IP3 Over Vdd in Gain Mode

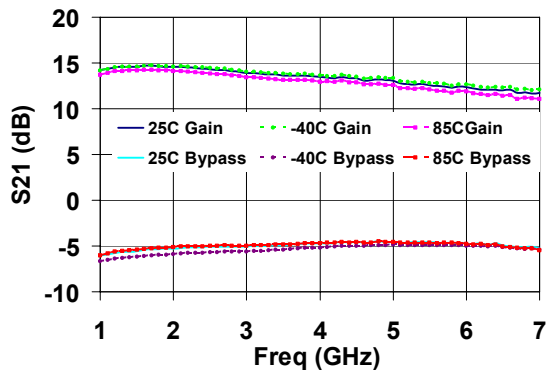


Figure 15. Gain over Temp

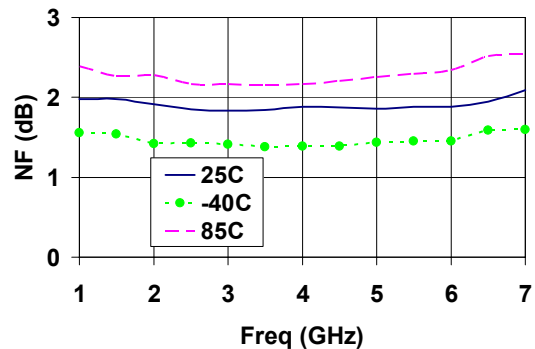


Figure 16 Noise Figure over Temp

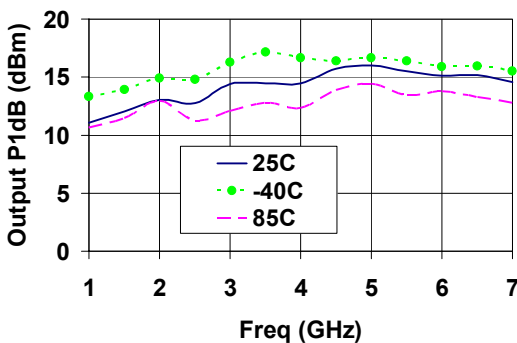


Figure 17. Output P1dB Over Temp in Gain Mode

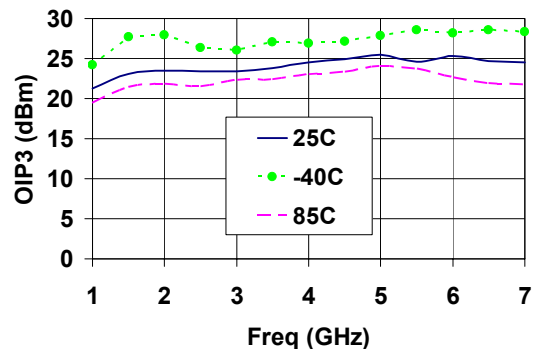


Figure 18. Output IP3 Over Temp In Gain Mode

Note:

[1] Over temp data are taken on a test fixture (Figure 20) without de-embedding

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VMMK-2103 Typical S-parameters in Gain State

(Data obtained using 300um G-S-G PCB substrate, losses calibrated out to the package reference plane;

$T_A = 25^\circ\text{C}$, $V_{dd}=5\text{V}$, $V_c=5\text{V}$, $I_{dd}=22\text{mA}$, $Z_{in} = Z_{out} = 50 \Omega$ unless noted)

Freq GHz	S11			S21			S12			S22		
	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase
0.1	-8.876	0.360	-50.581	16.829	6.942	176.611	-19.494	0.106	5.108	-9.404	0.339	-55.085
0.2	-12.270	0.244	-36.591	16.319	6.546	172.477	-19.584	0.105	0.002	-13.850	0.203	-43.101
0.3	-12.887	0.227	-30.174	16.117	6.395	169.661	-19.551	0.105	-3.117	-15.427	0.169	-33.218
0.4	-12.910	0.226	-28.995	16.006	6.314	167.231	-19.626	0.104	-4.633	-16.071	0.157	-26.579
0.5	-12.608	0.234	-21.522	15.848	6.200	168.339	-19.601	0.105	-3.401	-15.746	0.163	-10.589
0.9	-12.234	0.245	-31.690	15.684	6.084	161.128	-19.668	0.104	-7.506	-15.504	0.168	-3.349
1	-12.164	0.247	-34.073	15.658	6.066	159.287	-19.651	0.104	-8.499	-15.406	0.170	-2.282
1.5	-11.989	0.252	-49.198	15.480	5.943	150.058	-19.752	0.103	-13.093	-14.890	0.180	0.197
2	-11.839	0.256	-63.764	15.263	5.796	140.942	-19.845	0.102	-17.609	-14.329	0.192	0.774
2.5	-11.684	0.261	-77.546	15.033	5.645	132.079	-19.914	0.101	-22.064	-13.748	0.205	0.477
3	-11.535	0.265	-91.848	14.756	5.468	123.472	-20.052	0.099	-26.489	-13.124	0.221	0.527
3.5	-11.366	0.270	-103.974	14.488	5.301	115.038	-20.184	0.098	-31.117	-12.586	0.235	-1.231
4	-11.119	0.278	-115.567	14.209	5.134	106.819	-20.291	0.097	-35.608	-11.938	0.253	-4.965
4.5	-10.818	0.288	-126.554	13.943	4.979	98.880	-20.473	0.095	-40.251	-11.337	0.271	-8.749
5	-10.562	0.296	-137.192	13.658	4.818	90.999	-20.677	0.093	-44.626	-10.737	0.291	-12.668
5.5	-10.323	0.305	-146.916	13.380	4.667	83.237	-20.896	0.090	-49.245	-10.190	0.309	-17.172
6	-10.017	0.316	-156.605	13.113	4.525	75.640	-21.130	0.088	-54.220	-9.653	0.329	-21.621
6.5	-9.730	0.326	-166.084	12.844	4.387	68.093	-21.432	0.085	-58.831	-9.121	0.350	-26.308
7	-9.427	0.338	-175.142	12.580	4.256	60.663	-21.692	0.082	-63.579	-8.650	0.369	-31.224
7.5	-9.091	0.351	176.177	12.311	4.126	53.307	-22.047	0.079	-68.271	-8.210	0.389	-36.074
8	-8.745	0.365	167.300	12.054	4.006	45.851	-22.372	0.076	-73.024	-7.763	0.409	-41.086
8.5	-8.443	0.378	159.051	11.786	3.884	38.662	-22.745	0.073	-77.870	-7.333	0.430	-46.100
9	-8.070	0.395	150.995	11.524	3.769	31.423	-23.198	0.069	-83.171	-6.930	0.450	-51.449
9.5	-7.689	0.413	142.602	11.262	3.657	24.176	-23.649	0.066	-87.948	-6.575	0.469	-56.356
10	-7.329	0.430	134.912	10.992	3.545	16.891	-24.138	0.062	-93.302	-6.162	0.492	-61.479
10.5	-6.922	0.451	127.167	10.724	3.437	9.738	-24.642	0.059	-98.766	-5.833	0.511	-66.707
11	-6.549	0.471	119.700	10.449	3.330	2.475	-25.288	0.054	-104.531	-5.479	0.532	-71.957
11.5	-6.168	0.492	112.078	10.158	3.220	-4.775	-25.849	0.051	-110.478	-5.150	0.553	-77.110
12	-5.811	0.512	105.112	9.865	3.114	-11.968	-26.614	0.047	-115.827	-4.808	0.575	-82.407
12.5	-5.451	0.534	97.806	9.555	3.004	-19.144	-27.412	0.043	-121.940	-4.485	0.597	-87.740
13	-5.069	0.558	91.034	9.234	2.895	-26.308	-28.179	0.039	-128.028	-4.203	0.616	-92.835
13.5	-4.728	0.580	84.198	8.903	2.787	-33.415	-29.119	0.035	-135.270	-3.900	0.638	-98.017
14	-4.401	0.603	77.730	8.567	2.681	-40.569	-30.257	0.031	-143.074	-3.612	0.660	-103.148

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VMMK-2103 Typical S-parameters in Bypass State

(Data obtained using 300um G-S-G PCB substrate, losses calibrated out to the package reference plane;

$T_A = 25^\circ\text{C}$, $V_{dd}=5\text{V}$, $V_c=0\text{V}$, $I_{dd}=0.62\text{mA}$, $Z_{in} = Z_{out} = 50 \Omega$ unless noted)

Freq GHz	S11			S21			S12			S22		
	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase
0.1	-1.783	0.814	-28.679	-7.459	0.424	52.470	-7.488	0.422	52.351	-1.575	0.834	-26.461
0.2	-4.424	0.601	-42.034	-4.305	0.609	32.344	-4.329	0.608	32.536	-3.997	0.631	-39.454
0.3	-6.577	0.469	-46.955	-3.340	0.681	20.626	-3.359	0.679	20.936	-6.048	0.498	-44.552
0.4	-8.154	0.391	-48.467	-2.944	0.713	13.113	-2.952	0.712	13.388	-7.570	0.418	-46.186
0.5	-9.319	0.342	-44.468	-2.796	0.725	11.152	-2.796	0.725	11.316	-8.683	0.368	-42.316
0.9	-11.647	0.262	-42.225	-2.525	0.748	0.119	-2.534	0.747	0.318	-10.958	0.283	-39.530
1	-11.938	0.253	-41.789	-2.509	0.749	-1.784	-2.510	0.749	-1.634	-11.239	0.274	-38.886
1.5	-12.857	0.228	-43.145	-2.491	0.751	-9.483	-2.499	0.750	-9.319	-12.048	0.250	-39.139
2	-13.291	0.217	-46.787	-2.508	0.749	-15.778	-2.516	0.749	-15.569	-12.367	0.241	-41.755
2.5	-13.510	0.211	-51.914	-2.534	0.747	-21.385	-2.542	0.746	-21.281	-12.472	0.238	-45.429
3	-13.786	0.205	-58.267	-2.592	0.742	-26.797	-2.598	0.742	-26.724	-12.672	0.233	-50.016
3.5	-14.005	0.199	-64.423	-2.613	0.740	-32.019	-2.627	0.739	-31.925	-12.642	0.233	-55.405
4	-14.093	0.197	-71.644	-2.654	0.737	-37.161	-2.665	0.736	-37.053	-12.479	0.238	-59.927
4.5	-14.137	0.196	-79.054	-2.679	0.735	-42.193	-2.683	0.734	-42.150	-12.281	0.243	-64.996
5	-14.280	0.193	-87.252	-2.720	0.731	-47.296	-2.726	0.731	-47.196	-12.083	0.249	-70.218
5.5	-14.452	0.189	-95.034	-2.766	0.727	-52.335	-2.766	0.727	-52.294	-11.873	0.255	-75.476
6	-14.462	0.189	-103.880	-2.804	0.724	-57.423	-2.811	0.724	-57.354	-11.617	0.263	-80.534
6.5	-14.559	0.187	-113.166	-2.847	0.721	-62.558	-2.858	0.720	-62.499	-11.360	0.270	-85.294
7	-14.572	0.187	-122.733	-2.897	0.716	-67.739	-2.899	0.716	-67.657	-11.054	0.280	-90.818
7.5	-14.531	0.188	-132.794	-2.948	0.712	-72.905	-2.959	0.711	-72.847	-10.815	0.288	-95.990
8	-14.466	0.189	-143.549	-3.004	0.708	-78.235	-3.017	0.707	-78.118	-10.487	0.299	-101.093
8.5	-14.348	0.192	-153.759	-3.073	0.702	-83.500	-3.077	0.702	-83.352	-10.192	0.309	-106.034
9	-13.992	0.200	-164.621	-3.135	0.697	-88.876	-3.138	0.697	-88.811	-9.797	0.324	-111.230
9.5	-13.664	0.207	-176.432	-3.224	0.690	-94.404	-3.222	0.690	-94.284	-9.549	0.333	-116.425
10	-13.207	0.219	172.707	-3.305	0.684	-99.915	-3.301	0.684	-99.852	-9.196	0.347	-121.210
10.5	-12.631	0.234	161.575	-3.402	0.676	-105.528	-3.397	0.676	-105.465	-8.888	0.359	-126.564
11	-12.010	0.251	151.115	-3.510	0.668	-111.272	-3.501	0.668	-111.257	-8.573	0.373	-131.771
11.5	-11.415	0.269	140.472	-3.629	0.659	-117.082	-3.629	0.659	-117.046	-8.266	0.386	-136.822
12	-10.719	0.291	131.006	-3.768	0.648	-122.942	-3.773	0.648	-122.934	-7.946	0.401	-142.091
12.5	-10.072	0.314	121.223	-3.919	0.637	-128.970	-3.931	0.636	-128.910	-7.614	0.416	-147.433
13	-9.358	0.341	112.238	-4.096	0.624	-134.946	-4.105	0.623	-134.873	-7.383	0.427	-152.688
13.5	-8.678	0.368	103.491	-4.291	0.610	-141.009	-4.308	0.609	-140.922	-7.117	0.441	-157.942
14	-8.020	0.397	95.355	-4.501	0.596	-147.240	-4.521	0.594	-146.997	-6.878	0.453	-163.398

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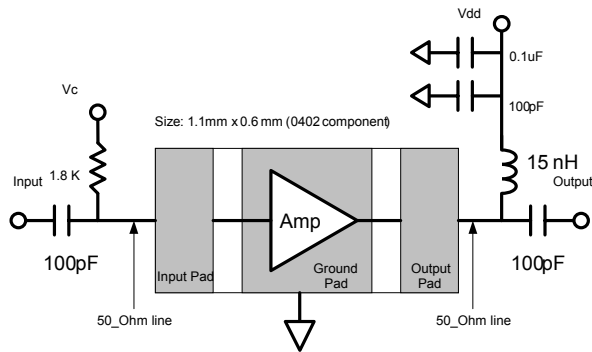


Figure 19. Example application of VMMK-2103 at 3GHz

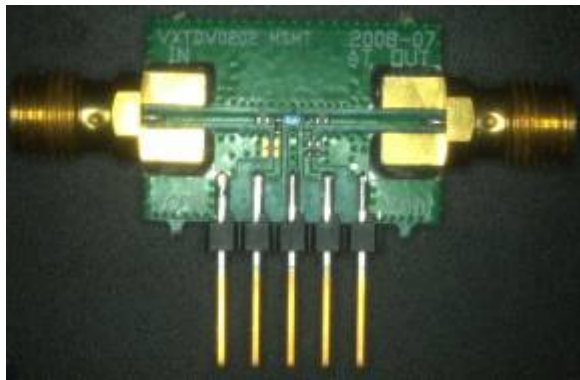


Figure 20. Evaluation/Test Board (available to qualified customer request)

Biasing and Operation

The VMMK-2103 can be used as a low noise amplifier or as a driver amplifier. The nominal bias condition for the VMMK-2103 is $V_d = V_c = 5V$. At this bias condition, the device provides an optimal compromise between power consumption, noise figure, gain, power output, and OIP3. The VMMK-2103 is biased with a positive supply connected to the output pin through an external user supplied bias-tee as shown in Figure 19. The bypass feature (V_c) at the input port is accessed through an external resistor. When V_c is 5V, the device is turned on. When V_c is at 0V, the device is biased in the “bypass” mode, which engages the integrated bypass switch while shuts down the amplifier.

In a typical application, the bias-tee on the output port can be constructed using lumped

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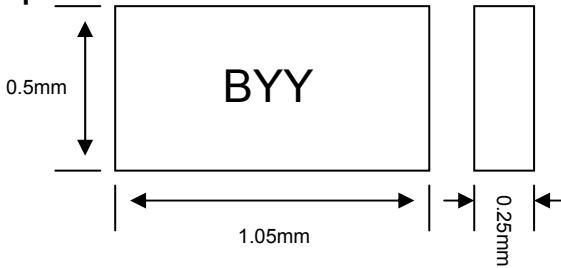
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elements. The value of the output inductor can have a major effect on both low and high frequency operation. The demo board uses a 15 nH inductor that has self resonant frequency higher than the maximum desired frequency of operation. If the self-resonant frequency of the inductor is too close to the operating band, the value of the inductor needs to be adjusted so that the self-resonant frequency is significantly higher than the highest frequency of operation. Extending the low frequency response of the VMMK-2103 is possible by using two different value inductors in series with the smaller value inductor placed closest to the device and favoring the higher frequencies. The larger value inductor will then offer better low frequency performance by not loading the output of the device. The parallel combination of the 100pF and 0.1uF capacitors provide a low impedance in the band of operation and at lower frequencies and should be placed as close as possible to the inductor. The low frequency bypass provides good rejection of power supply noise and also provides a low impedance termination for third order low frequency mixing products that will be generated when multiple in-band signals are injected into any amplifier. It is also suggested that a 0.1uF capacitor be used to bypass the resistor that feeds the V_c terminal. This will prevent noise and other spurious from effecting the noise figure of the VMMK-2103.

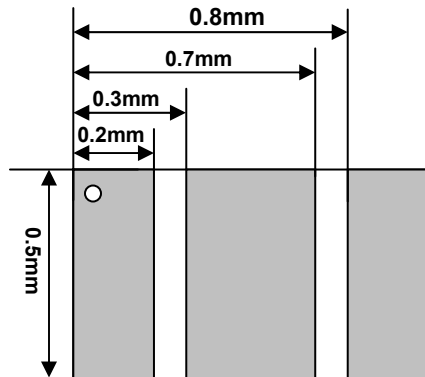
The value of the resistor that feeds the V_c terminal can have an impact in switching time. The demo board in Figure 20 uses a 1.8 Kohm resistor. Its switching time between the gain mode and bypass mode is approximately 2μsec. In application that desires faster switching time, an inductor can be used in place of the resistor. However, unlike a resistor, an inductor can limit the bandwidth of the device. For example, if a 22nH inductor is used to feed the V_c terminal (still using the same 15nH output inductor), the switching time is drastically reduced to under 0.1 μsec. Although above 1.5GHz, the two circuits perform the same, the one with the 22nH inductor is about 1dB lower in Gain at 1GHz compared to the one with the 1.8Kohm.

Outline Drawing

Top and Side View



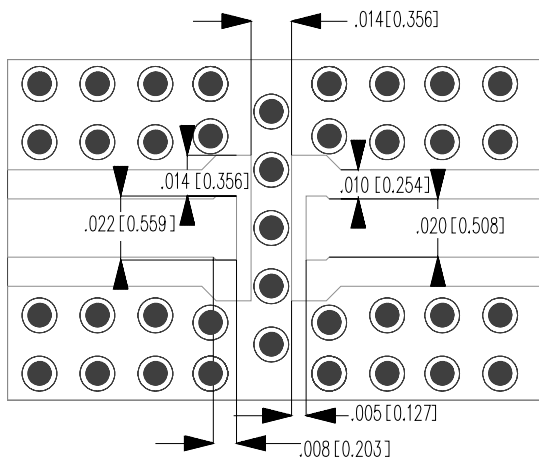
Bottom View



NOTES:

- indicates pin 1
- Dimensions are in millimeters
- Pad Material is minimum 5.0 um thick Au

Suggested PCB Material and Land Pattern



NOTES:

- 0.010" Rogers RO4350

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Recommended SMT Attachment

The VMMK Packaged Devices are compatible with high volume surface mount PCB assembly processes.

Manual Assembly for Prototypes

- Follow ESD precautions while handling packages.
- Handling should be along the edges with tweezers or from topside if using a vacuum collet.
- Recommended attachment is solder paste. Please see recommended solder reflow profile. Conductive epoxy is not recommended. Hand soldering is not recommended.
- Apply solder paste using either a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance. **Excessive solder will degrade RF performance.**
- Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temp to avoid damage due to thermal shock.
- Packages have been qualified to withstand a peak temperature of 280°C for 15 sec. Verify that the profile will not expose device beyond these limits.
- Clean off flux per vendor's recommendations.
- Clean the module with Acetone. Rinse with alcohol. Allow the module to dry before testing.



Note: These devices are ESD sensitive. The following precautions are strongly recommended. Ensure that an ESD approved carrier is used when die are transported from one destination to another.

Personal grounding is to be worn at all times when

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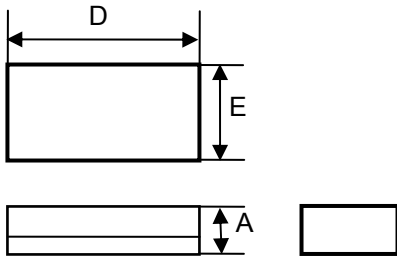
handling these devices. For more detail, refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control

ESD Machine Model (Class A)
ESD Human Body Model (Class A)

Ordering Information

Part Number	Devices Per Container	Container
VMMK-2403-BLKG	100	Antistatic Bag
VMMK-2403-TR1G	5000	7" Reel

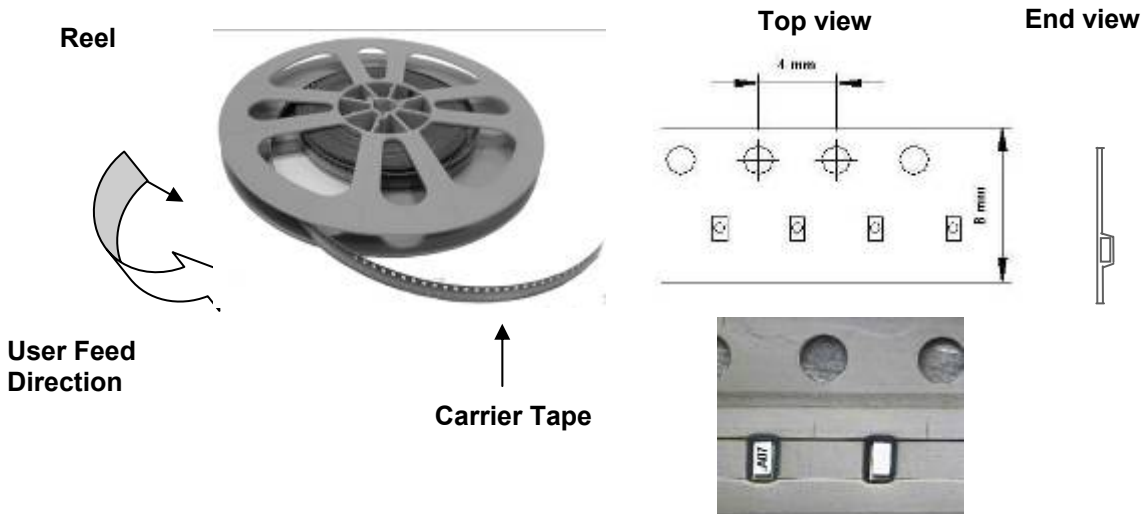
Package Dimension Outline



Dimensions		
Symbol	Min (mm)	Max (mm)
E	0.500	0.566
D	1.004	1.066
A	0.235	0.265

Note:
All dimensions are in mm

Device Orientation

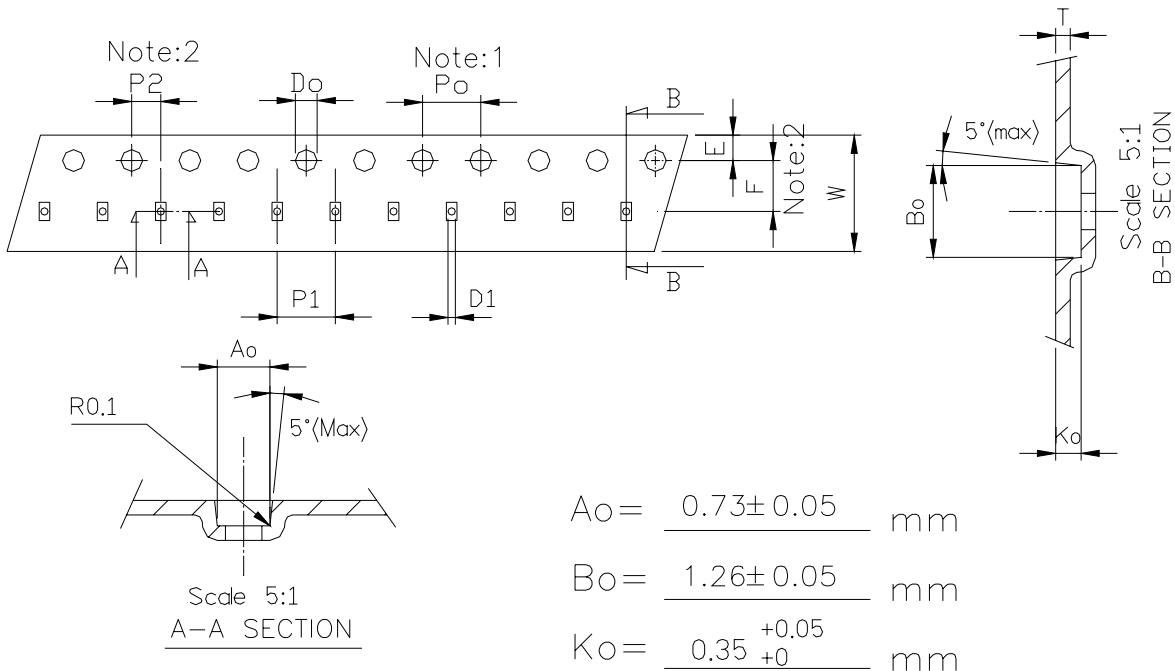


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$$A_0 = \frac{0.73 \pm 0.05}{\text{mm}}$$

$$B_0 = \frac{1.26 \pm 0.05}{\text{mm}}$$

$$K_0 = \frac{0.35^{+0.05}}{+0} \text{ mm}$$

Unit: mm

Symbol	Spec.
K1	-
P_0	4.0 ± 0.10
P_1	4.0 ± 0.10
P_2	2.0 ± 0.05
D_0	1.55 ± 0.05
D_1	0.5 ± 0.05
E	1.75 ± 0.10
F	3.50 ± 0.05
$10P_0$	40.0 ± 0.10
W	8.0 ± 0.20
T	0.20 ± 0.02

Notice:

1. 10 Sprocket hole pitch cumulative tolerance is $\pm 0.1\text{mm}$
2. Pocket position relative to sprocket hole measured as true position of pocket not pocket hole.
3. A_0 & B_0 measured on a plane 0.3mm above the bottom of the pocket to top surface of the carrier.
4. K_0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Carrier camber shall be not than 1mm per 100mm through a length of 250mm.

For product information and a complete list of Avago contacts and distributors, please go to our Website:

www.avagotech.com/semiconductors

E-mail: SemiconductorSupport@avagotech.com

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