VMMK-2203
0.9-11 GHz E-PHEMT Amplifier in a Wafer Scale Package

Preliminary Datasheet

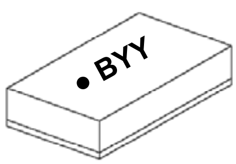
Description

Avago Technologies has combined its industry leading E-pHEMT technology with a revolutionary chip scale package.

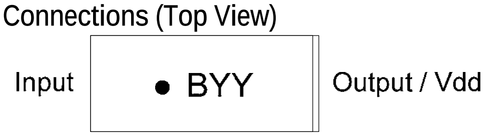
The VMMK-2203 is a easy-to-use GaAs MMIC amplifier that offers excellent gain and noise figure from 0.9 to 11 GHz. The input and output are matched to 50 Ω (better than 2:1 SWR) across the entire bandwidth so no external matching is needed. Bias is supplied through a simple external choke and DC blocking network.

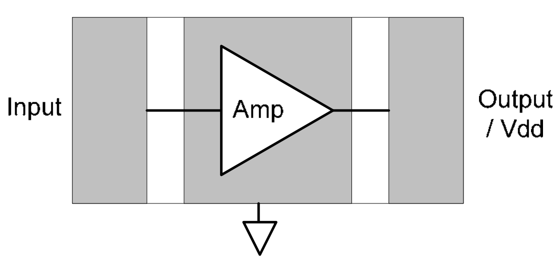
The wafer scale sub-miniature leadless package is small and ultra thin, yet can be handled and placed with standard 0402 pick and place assembly. This product is easy to use since it requires only a single positive DC voltage for bias and no matching coefficients are required for impedance matching to 50 Ω systems.

WaferCap™ 0402, 1mm x 0.5mm x 0.25 mm



Pin Connections (Top View)





Note:
"B" = Device Code
"YY" = Year Code

Features

- **Sub-miniature 0402 (1mm x 0.5mm) Surface Mount Leadless Package**
- **Low height (0.25mm)**
- **Frequency Range 0.9 to 11 GHz**
- **Enhancement Mode**
- **5 V Supply**
- **Tape and Reel packaging option available**

Specifications (5V, 25mA Typ.)

- **1.94dB typical noise figure**
- **16.5 dB available gain**
- **+14 dBm output 3rd order intercept**
- **+4 dBm output power**

Applications

- Low Noise and Driver for Cellular/PCS and WCDMA Base Stations
- 2.4 GHz, 3.5GHz, 5-6GHz WLAN and WiMax notebook computer, access point and mobile wireless applications
- 802.16 & 802.20 BWA systems
- WLL and MMDS Transceivers
- Point-to-Point Radio
- UWB
- Military Radar, radio and ECM systems

Attention:
Observe precautions for handling electrostatic sensitive devices.

ESD Machine Model (Class A)
ESD Human Body Model (Class 1A)
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control

Table 1. Absolute Maximum Ratings

Sym	Parameters/Condition	Unit	Absolute Max
Vd	Supply Voltage (RF Output)[2]	V	6.0
Id	Device Current)[2]	mA	50 mA
$P_{in, max}$	CW RF Input Power (RF Input))[3]	dBm	+15 dBm
P_{diss}	Total Power Dissipation	mW	300 mW
Tch	Max channel temperature	°C	+150
T_{STG}	Storage Temperature	°C	+150
θjc	Thermal Resistance)[4]	°C/W	107

Notes
1. Operation of this device above any one of these parameters may cause permanent damage
2. Bias is assumed DC quiescent conditions
3. With the DC (typical bias) and RF applied to the device at board temperature Tb= 25°C
4. Thermal resistance is measured from junction to board using IR method

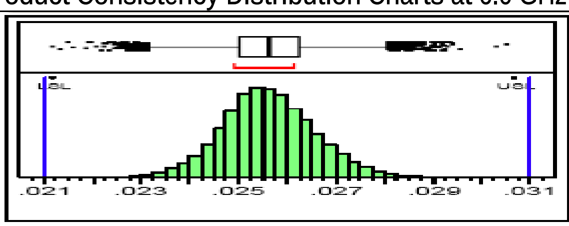
Table 2. DC and RF Specifications

T_A= 25°C, Frequency = 6 GHz, Vd = 5V , I_d=25mA, Z_{in}=Z_{out}=50Ω (unless otherwise specified)

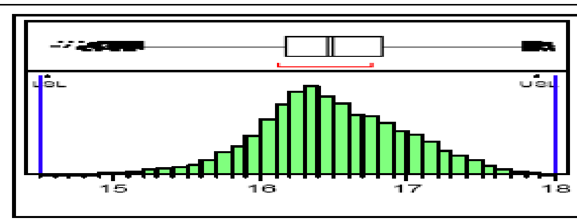
Sym	Parameters/Condition	Unit	Minimum	Typ.	Maximum
Id	Device Current	mA	21.0	25.6	31.0
NF[1,2]	Noise Figure	dB	-	1.94	2.3
Ga[1,2]	Associated Gain	dB	14.5	16.5	18.0
OIP3[1,2,3]	Output 3rd Order Intercept	dBm	+10	+14.0	-
P-1dB[1,2]	Output Power at 1dB Gain Compression (Pin = 0dBm)	dBm	+2.0	+5.0	-
IRL [1,2]	Input Return Loss	dB	-	-9.8	-
ORL [1,2]	Output Return Loss	dB	-	-9.8	-

Notes:
1. In test board, circuit losses have been de-embedded from actual measurements
2. Measure Data obtained using 300um G-S-G PCB substrate
3. OIP3 test condition: F1=6.0GHz, F2=6.01GHz, Pin=-20dB

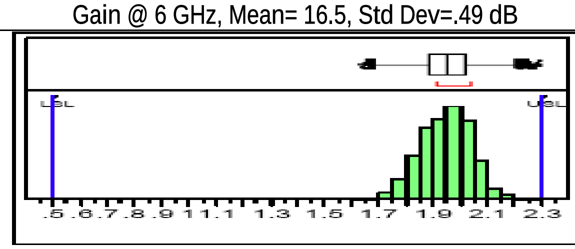
Product Consistency Distribution Charts at 6.0 GHz, Vd = 5 V



Id @ 3V, Mean= 25.6mA, Std Dev= 0.9mA



Gain @ 6 GHz, Mean= 16.5, Std Dev=.49 dB



NF @ 6 GHz, Mean= 1.94dB, Std Dev= .09dB

Note: Distribution data based on 500 part sample size from skew lots during initial characterization.

VMMK-2203 Typical Performance

(T_A = 25°C, Vdd=5V, Idd=25mA, Z_{in} = Z_{out} = 50 Ω unless noted;)

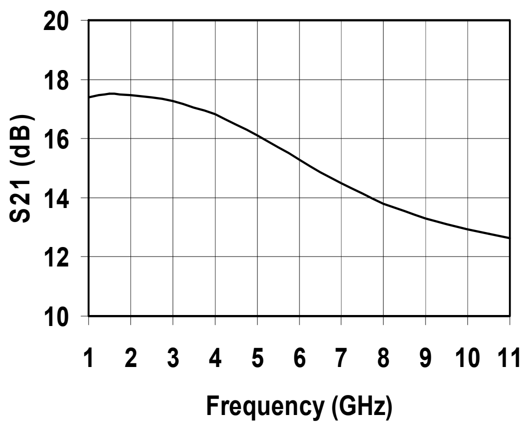


Figure 1. Small-signal Gain

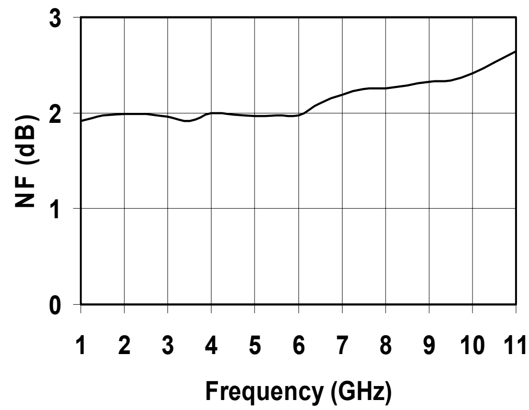


Figure 2. Noise Figure

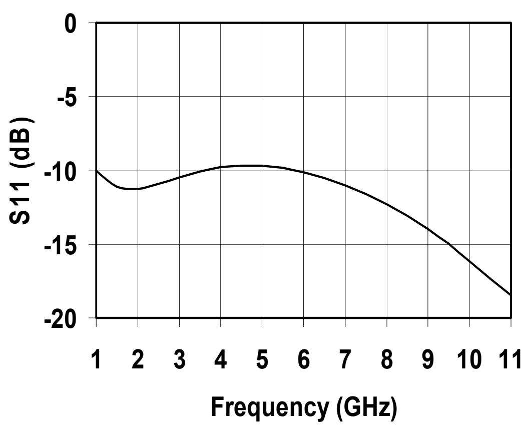


Figure 3. Input Return Loss

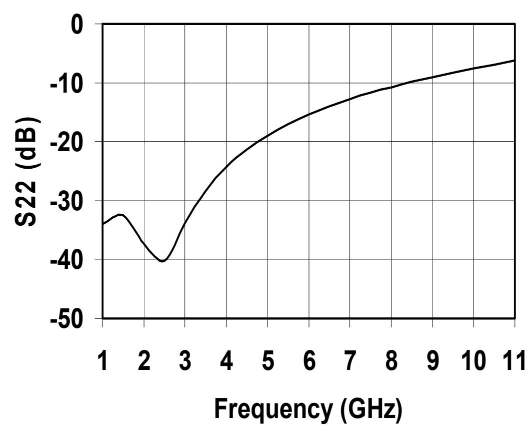


Figure 4. Output Return Loss

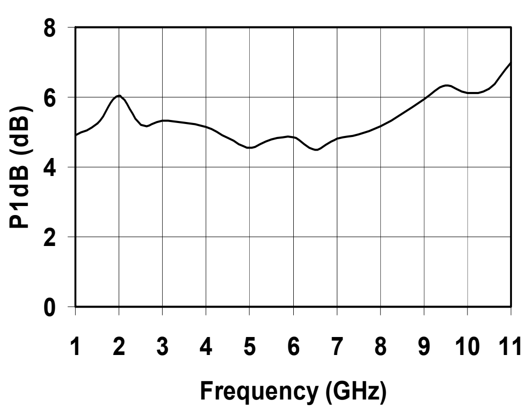


Figure 5. Output P-1dB

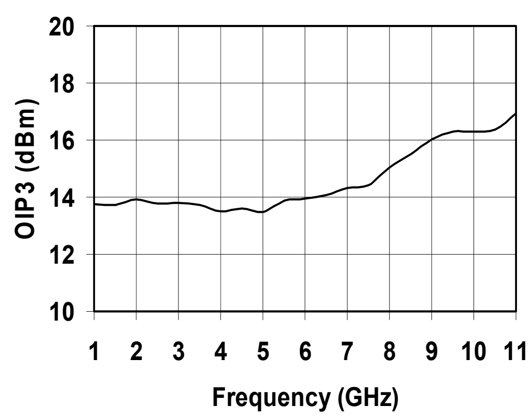


Figure 6. Output IP3

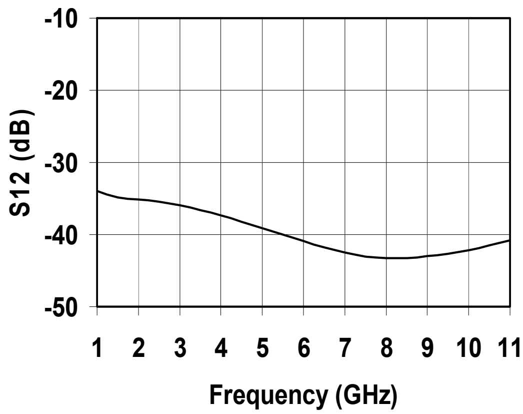


Figure 7. Isolation

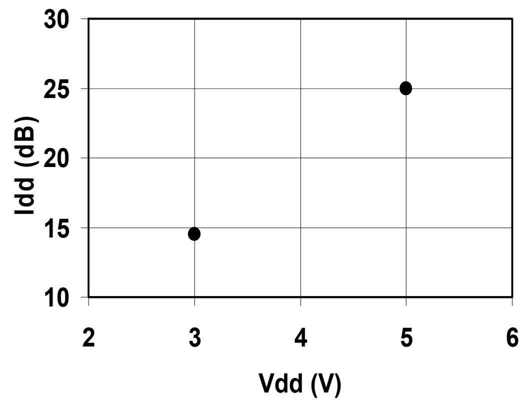


Figure 8. Total Current

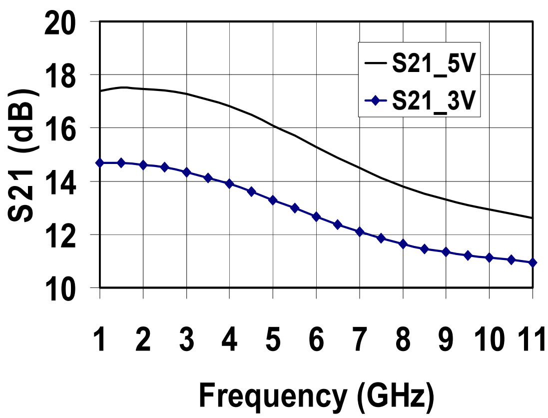


Figure 9. Gain over Vd

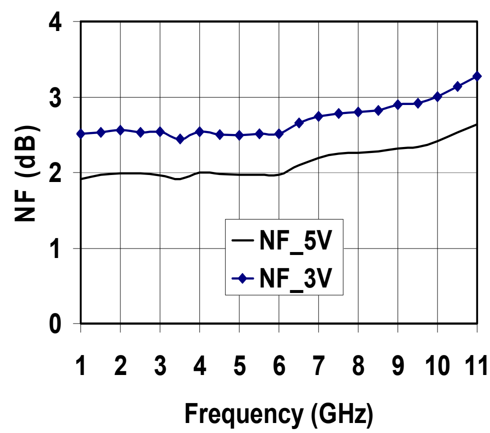


Figure 10 Noise Figure over Vd

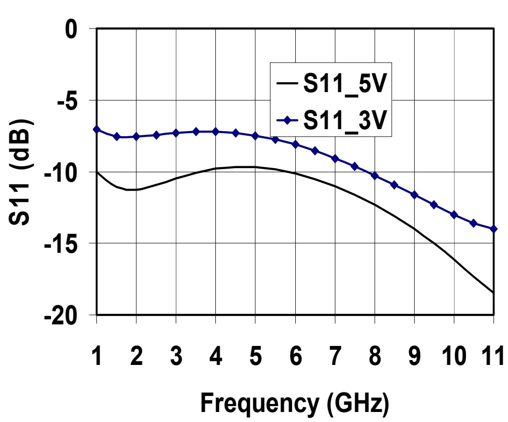


Figure 11. Input Return Loss Over Vdd

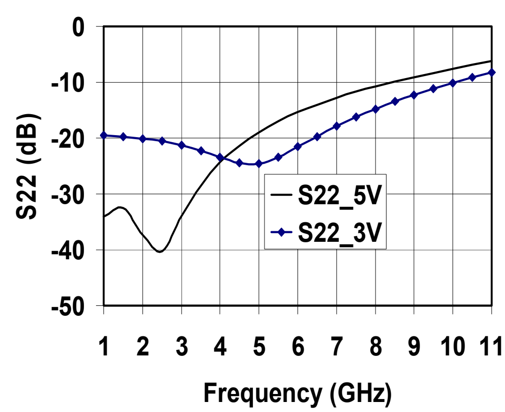


Figure 12. Output Return Loss Over Vdd

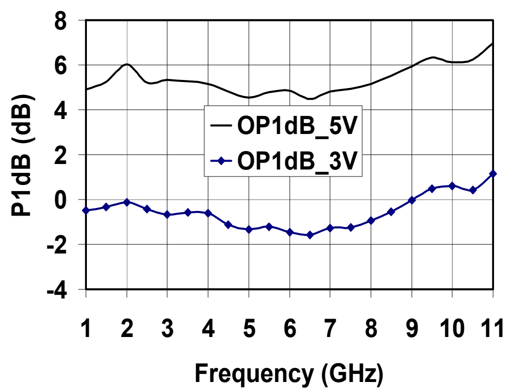


Figure 13. Output P-1dB over Vdd

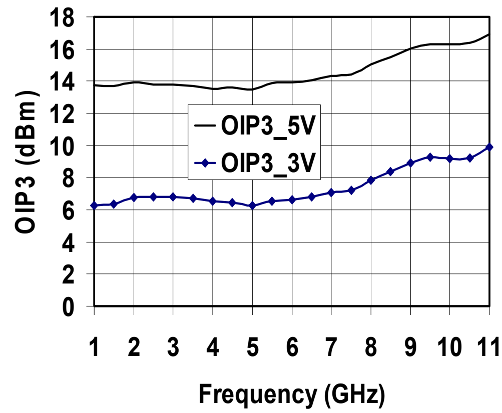


Figure 14. Output IP3 Over Vdd

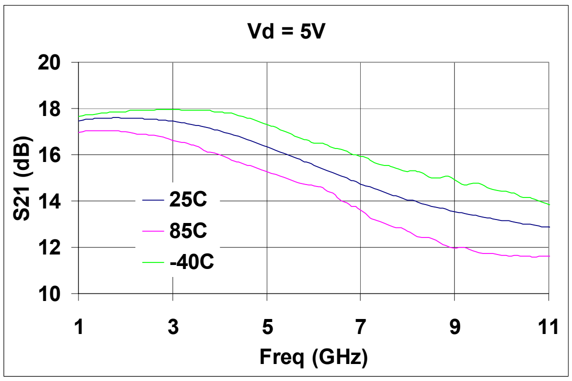


Figure 15. Gain over Temp

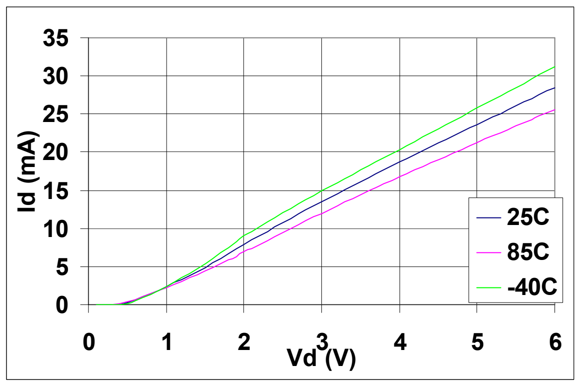


Figure 16 Idd over Temp

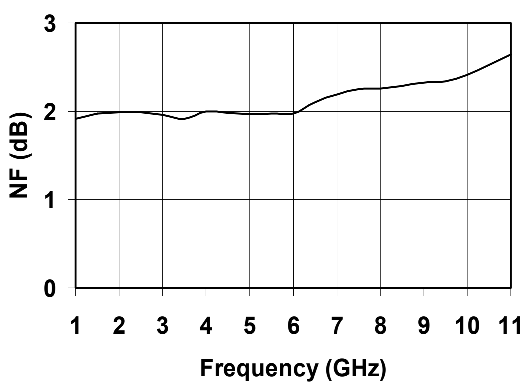


Figure 17. Noise Figure Over Temp

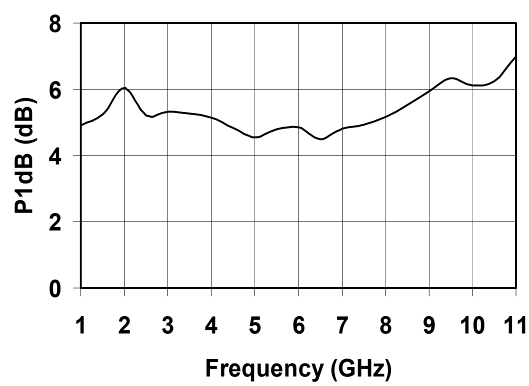


Figure 18. Output P1dB Over Temp

Typical Scattering Parameters

(Data obtained using 300um G-S-G PCB substrate, losses calibrated out to the package reference plane)

T_A = 25°C, V_{DD}=5V, I_{dq}=25mA, Z_{in}=Z_{out}=50Ω

Freq	S11			S21			S12			S22		
GHz	db	mag	Phase	db	mag	phase	db	mag	phase	db	mag	Phase
0.1	-0.623	0.931	-17.303	15.410	5.895	24.706	-43.098	0.007	58.201	-14.226	0.194	-60.924
0.2	-1.806	0.812	-30.763	16.296	6.528	11.177	-39.251	0.011	49.500	-18.666	0.117	-67.718
0.3	-3.217	0.691	-40.107	16.744	6.874	3.676	-37.202	0.014	38.074	-21.230	0.087	-71.757
0.4	-4.789	0.576	-42.585	16.937	7.028	0.281	-36.138	0.016	30.992	-25.224	0.055	-69.531
0.5	-6.014	0.500	-45.376	17.138	7.193	-4.222	-35.494	0.017	23.868	-27.013	0.045	-72.073
0.9	-9.520	0.334	-46.030	17.440	7.447	-19.422	-34.943	0.018	10.054	-32.841	0.023	-83.598
1	-10.053	0.314	-45.287	17.468	7.471	-22.849	-34.846	0.018	8.211	-34.657	0.019	-82.547
2	-11.859	0.255	-36.749	17.573	7.562	-54.672	-34.992	0.018	-7.465	-41.210	0.009	161.055
3	-11.242	0.274	-40.341	17.447	7.453	-85.386	-35.810	0.016	-16.631	-31.341	0.027	84.468
4	-10.554	0.297	-54.521	17.046	7.117	-115.626	-36.954	0.014	-23.677	-23.890	0.064	49.757
5	-10.446	0.300	-70.762	16.351	6.570	-144.946	-38.862	0.011	-26.344	-18.666	0.117	27.200
6	-10.989	0.282	-88.565	15.548	5.989	-172.420	-40.724	0.009	-25.092	-15.376	0.170	10.065
7	-11.965	0.252	-105.725	14.741	5.458	161.832	-42.158	0.008	-15.494	-13.046	0.223	-5.275
8	-13.267	0.217	-123.379	14.054	5.043	137.412	-43.098	0.007	-4.492	-11.179	0.276	-18.954
9	-14.919	0.180	-142.510	13.539	4.753	113.475	-42.853	0.007	8.295	-9.538	0.334	-31.497
10	-16.701	0.146	-166.823	13.159	4.550	89.158	-42.384	0.008	19.326	-8.011	0.398	-43.146
11	-17.972	0.126	163.087	12.879	4.405	63.721	-40.724	0.009	23.652	-6.616	0.467	-55.112
12	-17.781	0.129	128.897	12.543	4.238	36.160	-39.332	0.011	26.908	-5.338	0.541	-68.500
13	-16.496	0.150	97.602	11.875	3.924	6.410	-37.924	0.013	22.544	-4.465	0.598	-83.481
14	-14.943	0.179	72.431	10.617	3.395	-24.069	-37.788	0.013	14.404	-4.124	0.622	-98.826
15	-13.731	0.206	54.358	8.757	2.741	-53.104	-37.589	0.013	8.991	-4.278	0.611	-112.509
16	-12.597	0.235	40.489	6.512	2.116	-78.994	-37.856	0.013	6.710	-4.834	0.573	-123.438
17	-11.805	0.257	29.853	4.131	1.609	-101.974	-38.273	0.012	7.867	-5.430	0.535	-132.619
18	-10.906	0.285	20.369	1.789	1.229	-122.236	-38.416	0.012	4.077	-5.883	0.508	-139.697
19	-10.128	0.312	12.841	-0.460	0.948	-140.763	-38.862	0.011	3.017	-6.200	0.490	-145.124
20	-9.549	0.333	5.210	-2.569	0.744	-158.032	-39.412	0.011	-1.898	-6.375	0.480	-150.506

(Noise Parameters can be inserted here)

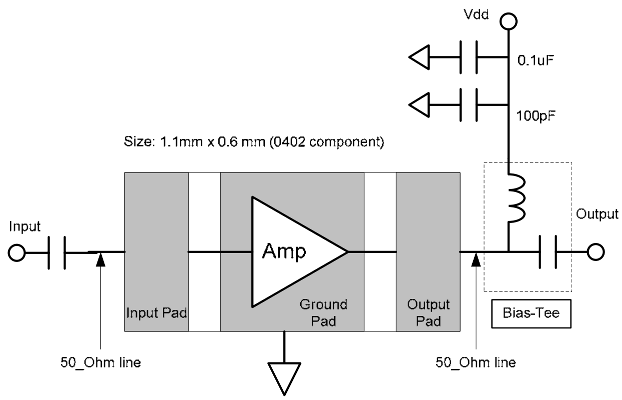


Figure 19. Usage of the VMMK-2203

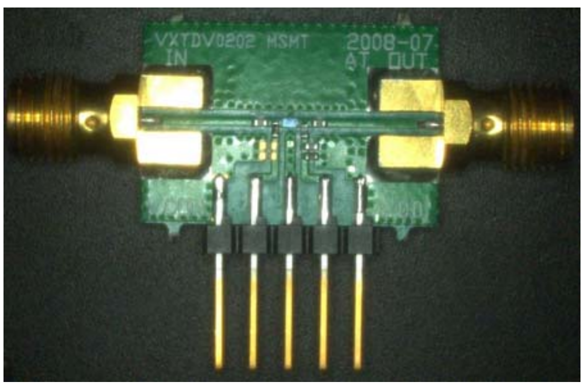


Figure 20. Evaluation/Test Board (available to qualified customer request)

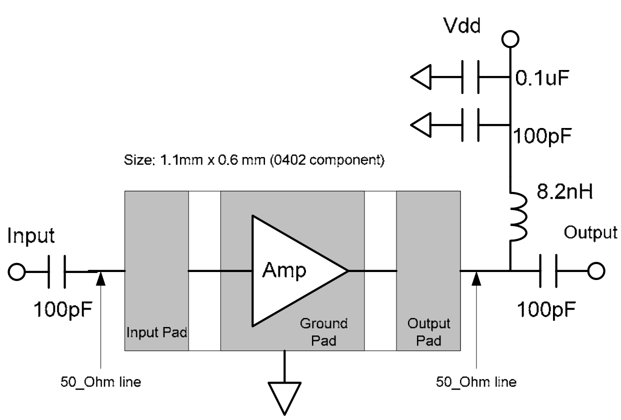


Figure 21. Example application of VMMK-2203

Biasing and Operation

The VMMK-2203 is normally biased with a positive drain supply connected to the output pin through an external bias-tee and with bypass capacitors as shown in **Figure 19**. The recommended drain supply voltage is 5 V and the corresponding drain current is approximately 25mA. It is important to have 0.1uF and 100pF bypass capacitors and the capacitors should be placed as close to the component as possible. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity, or low noise (Γopt) matching.

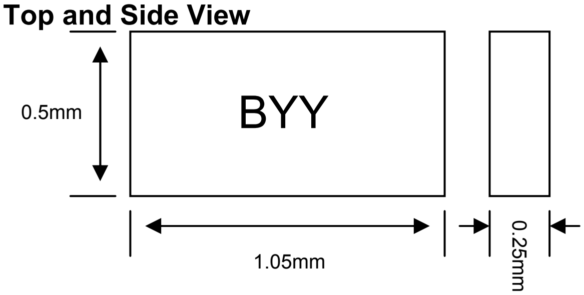
The external bias-tee can be built using an inductor of 15nH and a capacitor of 100pF. Different manufacturers have different self-resonant frequencies for the 15nH inductor. If the self-resonant frequency is too close to the operating frequency band, the value of the bias-tee's inductor needs to be adjusted so that the self-resonant frequency is significantly higher than highest frequency specified (11GHz).

The VMMK-2203 can also be safely biased at 3V or 5V as desired. At 5V, the performance is an optimal compromise between power consumption, noise figure, gain and power/linearity. It is both applicable to be used as a low noise block or driver. At 3V and 5V, it draws about 15mA and 25mA respectively. At higher Vdd, the amplifier can provide 1 to 2dBm more output power for LO or transmitter driver applications where high output power and linearity are often required.

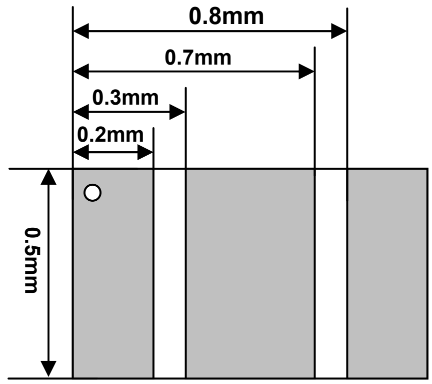
Refer the Absolute Maximum Ratings table for allowed DC and thermal conditions.

Outline Drawing

Top and Side View



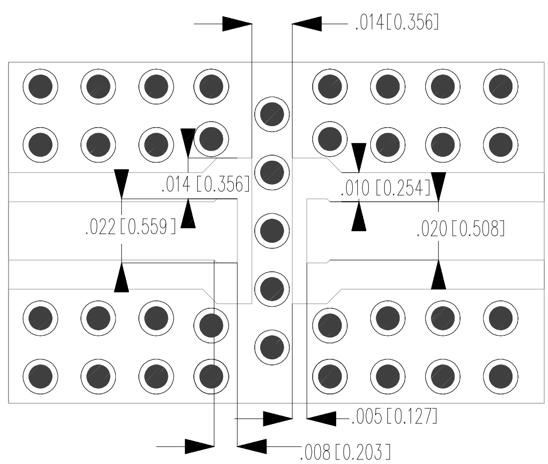
Bottom View



NOTES:

1. • indicates pin 1
2. Dimensions are in millimeters
3. Pad Material is minimum 5.0 um thick Au

Suggested PCB Material and Land Pattern



NOTES:

1. 0.010" Rogers RO4350

Recommended SMT Attachment

The VMMK Packaged Devices are compatible with high volume surface mount PCB assembly processes.

<u>Manual Assembly for Prototypes</u>

1. Follow ESD precautions while handling packages.
2. Handling should be along the edges with tweezers or from topside if using a vacuum collet.
3. Recommended attachment is solder paste. Please see recommended solder reflow profile. Conductive epoxy is not recommended. Hand soldering is not recommended.
4. Apply solder paste using either a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance. ***Excessive solder will degrade RF performance.***
5. Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temp to avoid damage due to thermal shock.
6. Packages have been qualified to withstand a peak temperature of 280°C for 15 sec. Verify that the profile will not expose device beyond these limits.
7. Clean off flux per vendor's recommendations.
8. Clean the module with Acetone. Rinse with alcohol. Allow the module to dry before testing.

Note: These devices are ESD sensitive. The following precautions are strongly recommended. Ensure that an ESD approved carrier is used when die are transported from one destination to another. Personal grounding is to be worn at all times when handling these devices. For more detail, refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control

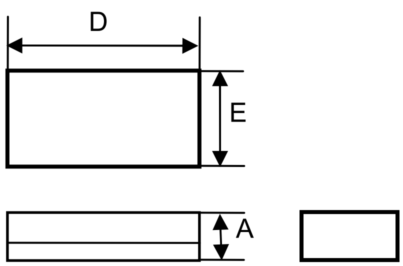
ESD Machine Model (Class A)

ESD Human Body Model (Class A)

Ordering Information

Part Number	Devices Per Container	Container
VMMK-2403-BLKG	100	Antistatic Bag
VMMK-2403-TR1G	5000	7" Reel

Package Dimension Outline

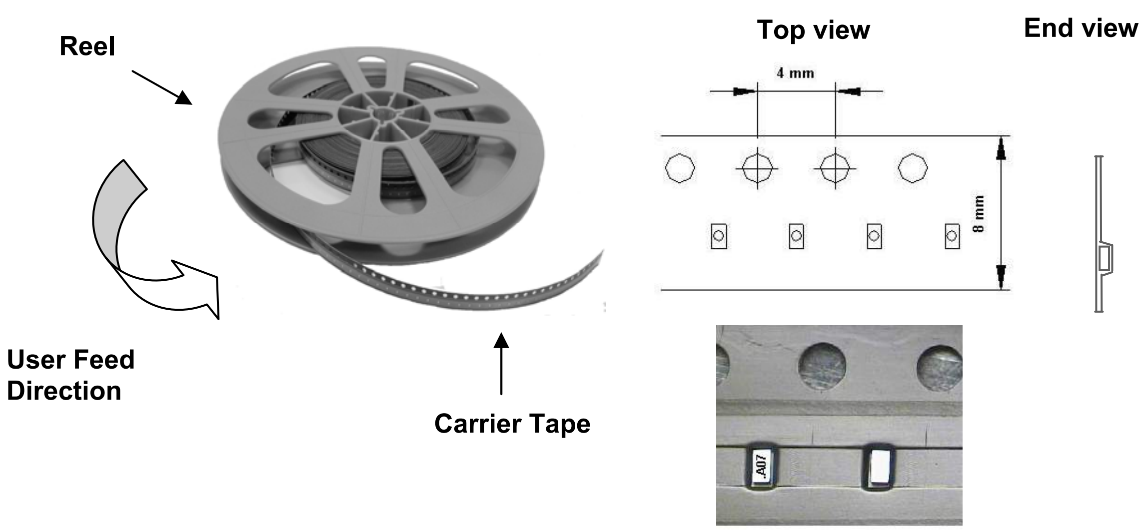


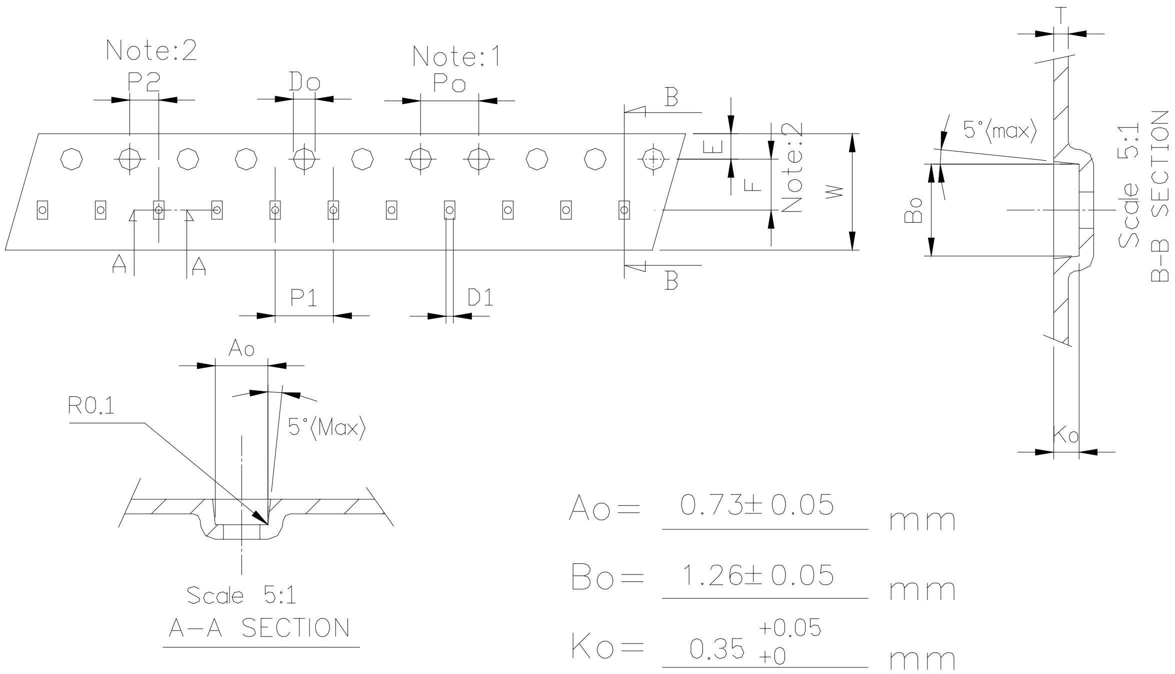
Dimensions

Symbol	Min (mm)	Max (mm)
E	0.500	0.566
D	1.004	1.066
A	0.235	0.265

Note:
All dimensions are in mm

Device Orientation





Unit: mm

Symbol	Spec.
K1	–
Po	4.0± 0.10
P1	4.0± 0.10
P2	2.0± 0.05
Do	1.55± 0.05
D1	0.5± 0.05
E	1.75± 0.10
F	3.50± 0.05
10Po	40.0± 0.10
W	8.0± 0.20
T	0.20± 0.02

Notice:

1. 10 Sprocket hole pitch cumulative tolerance is ± 0.1mm
2. Pocket position relative to sprocket hole measured as true position of pocket not pocket hole.
3. Ao & Bo measured on a place 0.3mm above the bottom of the pocket to top surface of the carrier.
4. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Carrier camber shall be not than 1mm per 100mm through a length of 250mm.

For product information and a complete list of Avago contacts and distributors, please go to our Website: www.avagotech.com/semiconductors
*E-mail:*SemiconductorSupport@avagotech.com
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