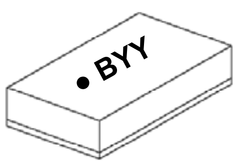
VMMK-2303
0.5 to 6 GHz 1.8 Volts GaAs LNA in Wafer Scale Package

Preliminary Datasheet

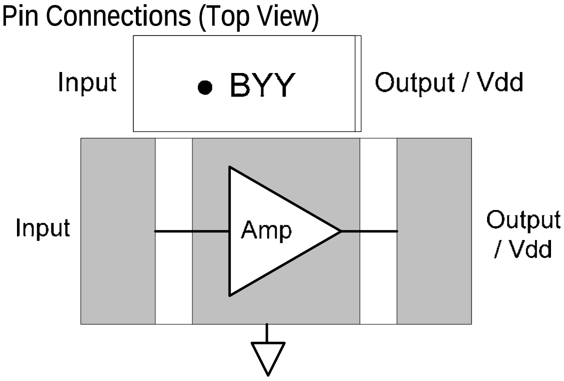
Description

Avago's VMMK-2303 is an easy-to-use GaAs MMIC amplifier that offers excellent noise figure and flat gain from 0.5 to 6 GHz in a miniaturized wafer-scale SMT package. It operates from 1.8V CMOS supply or 3.3V battery supply. The bias circuit is fitted with a power down feature which is accessed from the input port by way of a large value external resistor. The input and output are matched to 50 Ω (better than 2:1 SWR) across the entire bandwidth; no external matching is needed. This amplifier is fabricated with enhancement E-pHEMT technology and industry leading revolutionary chip scale package. The GaAsCap wafer scale sub-miniature leadless package is small and ultra thin yet can be handled and placed with standard 0402 pick and place assembly.

WaferCap™ 0402, 1mm x 0.5mm x 0.25 mm



Pin Connections (Top View)



Note:
"B" = Device Code
"YY" = Year Code

Features

- **1 x 0.5 mm Surface Mount Package**
- **Low height (0.25mm)**
- **Power down function**
- **1.8V Supply**
- **50Ohm Input and Output Match**

Specifications (1.8V, 20mA Typ.)

- **< 2.2dB noise figure**
- **13dB available gain**
- **1.5dB gain flatness (0.5 to 6 GHz)**
- **22 dBm output 3rd order intercept**
- **9 dBm output power**

Applications

- Low Noise and Driver for Cellular/PCS and WCDMA Base Stations
- 2.4 GHz, 3.5GHz, 5-6GHz WLAN and WiMax notebook computer, access point and mobile wireless applications
- 802.16 & 802.20 BWA systems
- WLL and MMDS Transceivers
- Military Radar, radio and ECM systems

Attention:
Observe precautions for handling electrostatic sensitive devices.

ESD Machine Model (Class A)
ESD Human Body Model (Class 1A)
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control

Table 1. Absolute Maximum Ratings

Sym	Parameters/Condition	Unit	Absolute Max
Vd	Supply Voltage (RF Output)[2]	V	5.0
Vc	Power Down Control Voltage	V	3.3
Id	Device Current)[2]	mA	60 mA
$P_{in, max}$	CW RF Input Power (RF Input))[3]	dBm	+5 dBm
P_{diss}	Total Power Dissipation	mW	300 mW
Tch	Max channel temperature	$_o$C	+150
T_{STG}	Storage Temperature	°C	+150
Θjc	Thermal Resistance)[4]	°C/W	140

Notes
1. Operation of this device above any one of these parameters may casue permanment damage
2. Bias is assumed DC quiescent conditions
3. With the DC (typical bias) and RF applied to the device at board temperature Tb= 25°C
4. Thermal resistance is measured from junction to board using IR method

Table 2. DC and RF Specifications
T_A= 25°C, Frequency = 6 GHz, Vd = 1.8V, Vc=1.8V, I_d=21mA, Z_{in}=Z_{out}=50Ω (unless otherwise specified)

Sym	Parameters/Condition	Unit	Minimum	Typ.	Maximum
Id	Device Current	mA	15	20.7	25
Id_leakage	Current in Shut Down Mode	μA		0.05	10
NF[1,2]	Noise Figure	dB	-	1.86	2.5
Ga[1,2]	Associated Gain	dB	12.5	14.1	15.5
OIP3[1,2,3]	Output 3rd Order Intercept	dBm		+22	-
P-1dB[1,2]	Output Power at 1dB Gain Compression	dBm		+9	-
IRL [1,2]	Input Return Loss	dB	-	-11	-
ORL [1,2]	Output Return Loss	dB	-	-11	-

Notes:
1. In test board, circuit losses have been de-embedded from actual measurements
2. Measure Data obtained using 300um G-S-G PCB substrate
3. OIP3 test condition: F1=6.0GHz, F2=6.01GHz, Pin=-20dB

Product Consistency Distribution Charts at 6.0 GHz, Vd = 1.8 V, Vc=1.8V

Id @ Vd=Vc=1.8V, Mean=, Std Dev=	Gain @ 6 GHz, Mean= , Std Dev=
Id_off @Vd=1.8V, Vc=0V, Mean, Std Dev=	NF @ 6 GHz, Mean= , Std Dev=

Note: Distribution data based on 500 part sample size from skew lots during initial characterization.

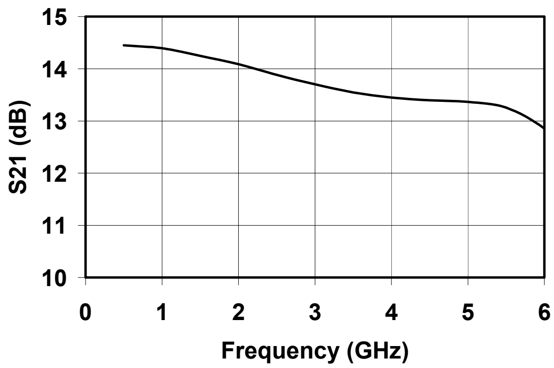


Figure 1. Small-signal Gain

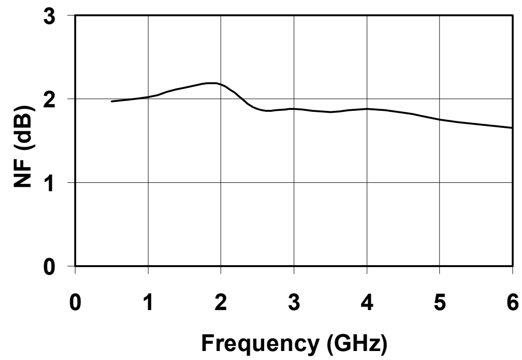


Figure 2. Noise Figure

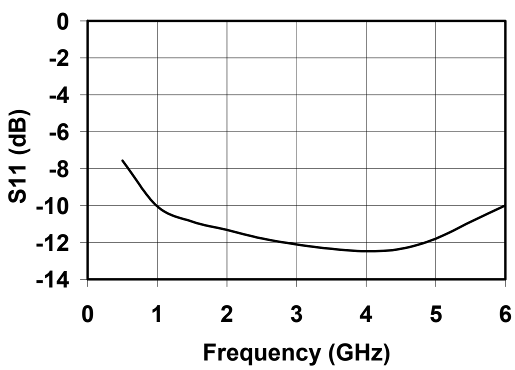


Figure 3. Input Return Loss

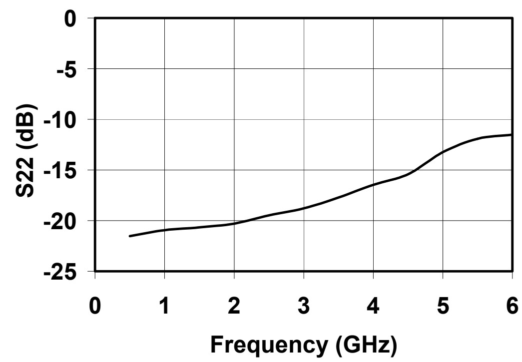


Figure 4. Output Return Loss

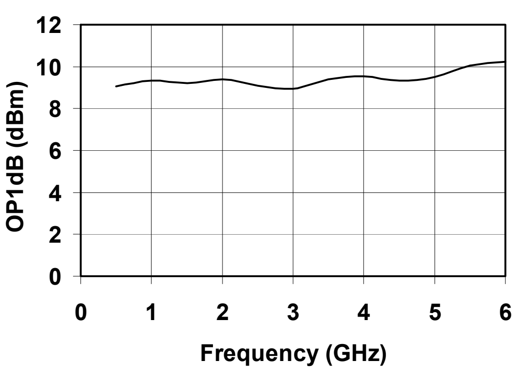


Figure 5. Output P-1dB

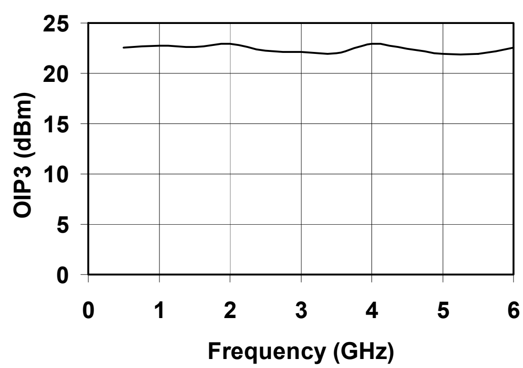


Figure 6. Output IP3

Note:
[1] S-parameters are measured on a fully de-embeded test fixture
[2] Noise Figure is measured on a fully de-embeded test fixture in 50-Ohm environment

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(T_A = 25°C, Vdd=1.8V, Vc=1.8V, Idd=21mA, Z_{in} = Z_{out} = 50 Ω unless noted)

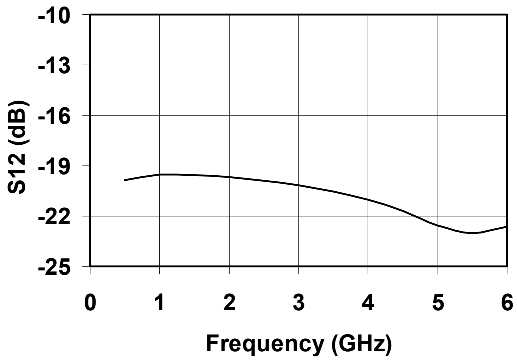

Figure 7. Isolation

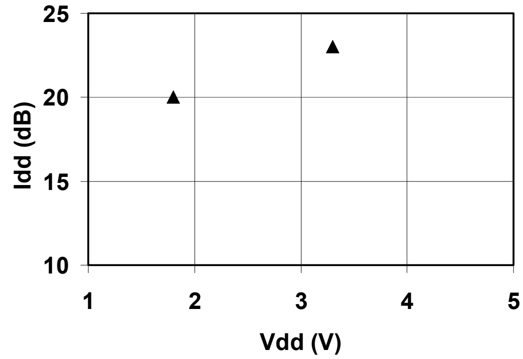

Figure 8. Total Current

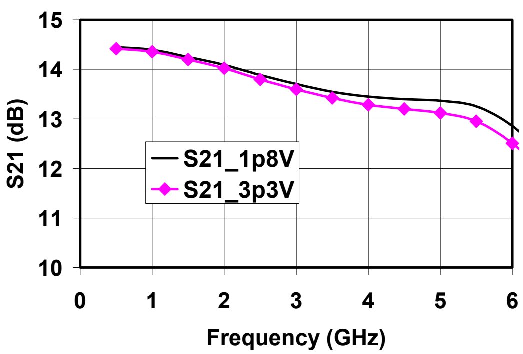

Figure 9. Gain over Vdd

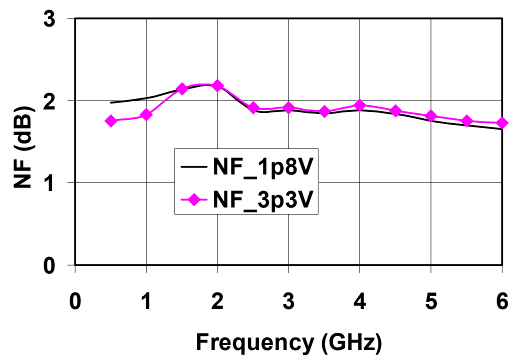

Figure 10 Noise Figure over Vdd

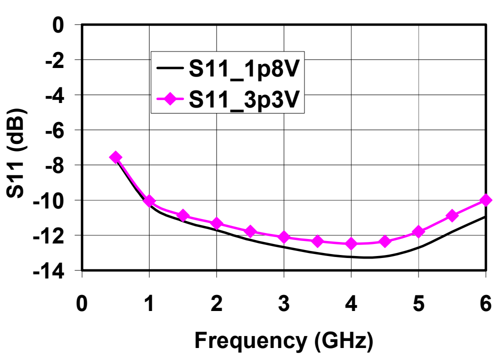

Figure 11. Input Return Loss Over Vdd

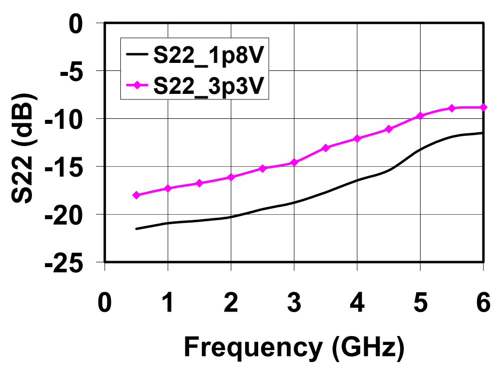

Figure 12. Output Return Loss Over Vdd

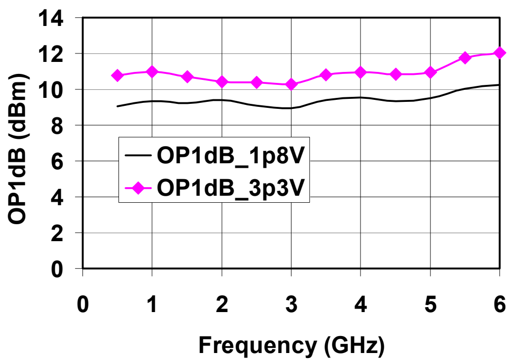

Figure 13. Output P-1dB over Vdd

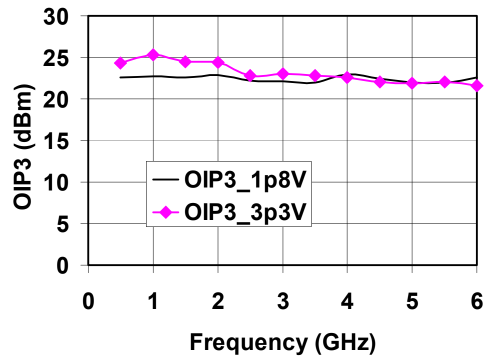

Figure 14. Output IP3 Over Vdd

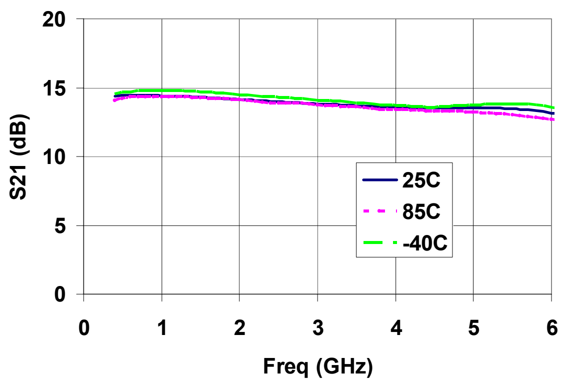

Figure 15. Gain over Temp

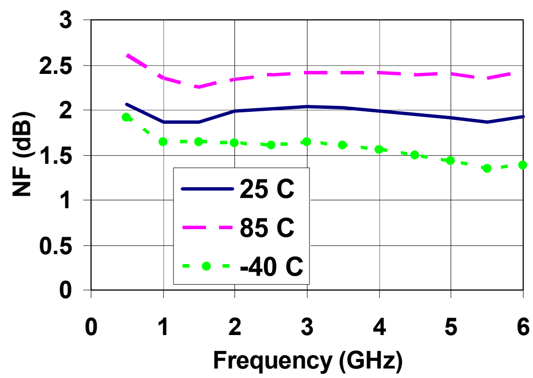

Figure 16 Noise Figure over Temp

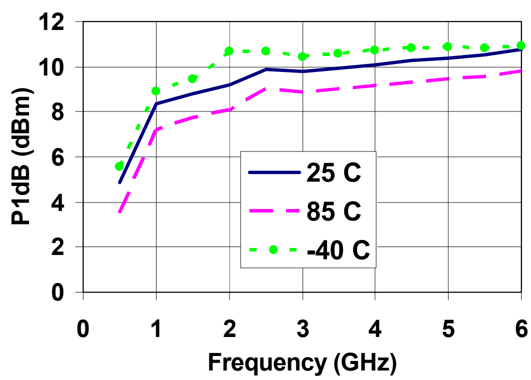

Figure 17. P1dB Over Temp

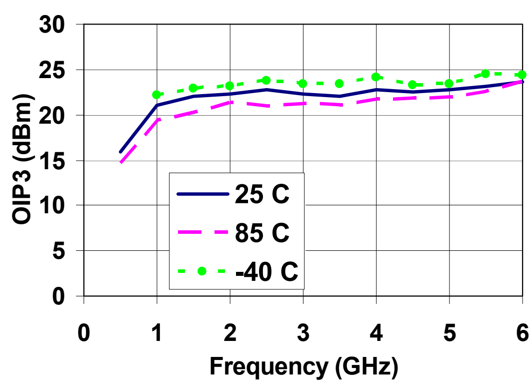

Figure 18. Output IP3 Over Temp

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VMMK-2303 Typical S-parameters

(Data obtained using 300um G-S-G PCB substrate, losses calibrated out to the package reference plane; T_A = 25°C, Vdd=1.8V, Vc=1.8V, Idd=21mA, Z_{in} = Z_{out} = 50 Ω unless noted)

Freq	S11			S21			S12			S22		
GHz	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase
0.1	-1.189	0.872	-25.218	13.588	4.780	-178.071	-25.597	0.053	59.673	-28.754	0.037	102.740
0.2	-3.285	0.685	-40.252	14.034	5.032	178.844	-21.873	0.081	39.048	-24.013	0.063	56.683
0.3	-5.171	0.551	-48.030	14.274	5.173	175.178	-20.621	0.093	25.793	-22.476	0.075	36.971
0.4	-6.965	0.449	-48.479	14.334	5.209	174.141	-20.114	0.099	20.372	-20.819	0.091	43.571
0.5	-8.033	0.397	-49.998	14.383	5.238	171.490	-19.862	0.102	14.988	-20.734	0.092	34.642
0.9	-10.340	0.304	-55.088	14.389	5.241	161.829	-19.502	0.106	2.738	-20.602	0.093	17.406
1	-10.633	0.294	-56.660	14.355	5.221	159.550	-19.469	0.106	0.569	-20.327	0.096	14.799
1.5	-11.604	0.263	-66.322	14.237	5.151	148.646	-19.510	0.106	-7.764	-20.247	0.097	5.593
2	-12.465	0.238	-77.367	14.066	5.050	138.043	-19.609	0.105	-14.262	-20.455	0.095	-4.429
2.5	-13.120	0.221	-92.069	13.921	4.967	127.967	-19.777	0.103	-20.126	-19.854	0.102	-10.667
3	-13.756	0.205	-105.553	13.761	4.876	117.996	-20.044	0.100	-25.917	-19.315	0.108	-16.656
3.5	-14.080	0.198	-121.275	13.625	4.800	108.216	-20.355	0.096	-31.482	-18.577	0.118	-19.883
4	-14.164	0.196	-138.080	13.528	4.747	98.536	-20.819	0.091	-36.539	-17.215	0.138	-24.628
4.5	-14.080	0.198	-155.711	13.469	4.715	88.588	-21.473	0.084	-41.043	-15.682	0.164	-28.934
6	-10.734	0.291	137.934	13.064	4.500	53.142	-22.639	0.074	-39.719	-11.962	0.252	-67.155
6.5	-9.789	0.324	112.577	12.421	4.179	41.188	-21.971	0.080	-42.502	-12.385	0.240	-84.103
7	-9.114	0.350	90.524	11.686	3.840	30.984	-21.598	0.083	-49.096	-13.416	0.213	-97.269
7.5	-8.552	0.374	71.896	11.011	3.553	21.893	-21.639	0.083	-56.813	-14.572	0.187	-106.937
8	-7.985	0.399	55.866	10.407	3.314	13.237	-21.927	0.080	-64.022	-15.783	0.163	-114.375
8.5	-7.414	0.426	41.571	9.855	3.110	4.832	-22.395	0.076	-71.213	-16.936	0.142	-119.103
9	-6.934	0.450	28.414	9.336	2.930	-3.596	-22.987	0.071	-78.204	-18.048	0.125	-123.159
9.5	-6.519	0.472	16.304	8.820	2.761	-12.097	-23.702	0.065	-85.057	-19.188	0.110	-125.957
10	-6.152	0.493	5.143	8.292	2.598	-20.481	-24.539	0.059	-92.301	-20.175	0.098	-128.274
10.5	-5.857	0.510	-5.889	7.753	2.442	-28.823	-25.449	0.053	-98.980	-21.412	0.085	-129.273
11	-5.698	0.519	-16.421	7.207	2.293	-37.155	-26.558	0.047	-106.295	-22.418	0.076	-129.884
11.5	-5.647	0.522	-26.546	6.634	2.146	-45.392	-27.894	0.040	-114.058	-23.504	0.067	-129.694
12	-5.668	0.521	-36.450	6.034	2.003	-53.627	-29.499	0.034	-122.428	-24.657	0.059	-128.305
12.5	-5.769	0.515	-46.265	5.403	1.863	-61.689	-31.437	0.027	-131.444	-25.900	0.051	-125.420
13	-6.024	0.500	-56.018	4.750	1.728	-69.652	-33.893	0.020	-143.164	-26.859	0.045	-119.561
13.5	-6.384	0.480	-65.570	4.058	1.596	-77.410	-36.954	0.014	-157.876	-27.597	0.042	-113.832
14	-6.786	0.458	-74.640	3.346	1.470	-84.974	-40.537	0.009	176.577	-28.382	0.038	-107.341

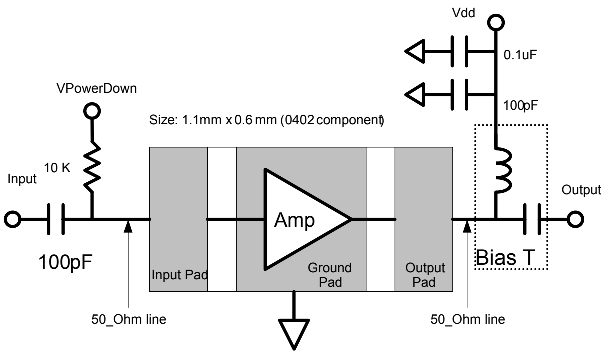


Figure 19. Usage of the VMMK-2303

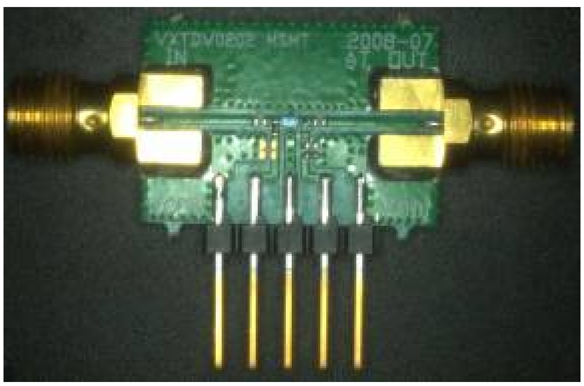


Figure 20. Evaluation/Test Board (available to qualified customer request)

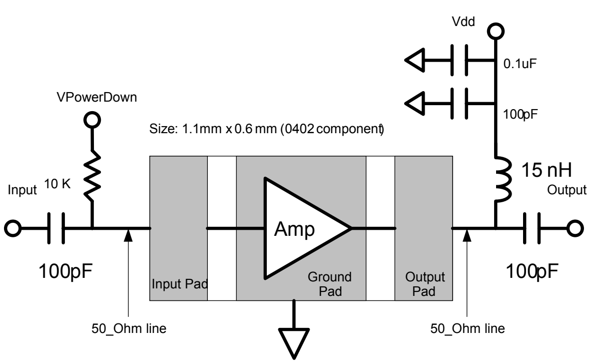


Figure 21. Example application of VMMK-2303 at 3GHz

Biasing and Operation

The VMMK-2303 is normally biased with a positive drain supply connected to the output pin through an external bias-tee and with bypass capacitors as shown in **Figure 19**. The power down feature is accessed from the input port by way a 10K ohm external resistor. The recommended drain supply voltage is 1.8 V and control voltage is 1.8V. Its corresponding drain current is approximately 21mA. It is important to have 0.1uF and 100pF bypass capacitors and the capacitors should be placed as close to the component as possible. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity, or low noise (Γopt) matching.

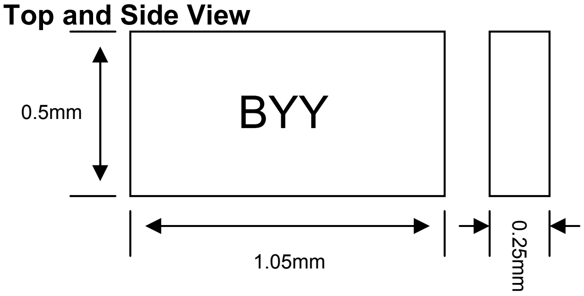
The external bias-tee can be built using an inductor of 15nH and a capacitor of 100pF. Different manufacturers have different self-resonant frequencies for the 15nH inductor. If the self-resonant frequency is too close to the operating frequency band, the value of the bias-tee's inductor needs to be adjusted so that the self-resonant frequency is significantly higher than highest frequency specified (6GHz).

At Vdd and Vc at 1.8V, the performance is an optimal compromise between power consumption, noise figure, gain and power/linearity. It is both applicable to be used as a low noise block or driver. The VMMK-2303 can also be safely biased at 3.3V Vdd and 1.8V Vc as desired. At higher Vdd (but still keep Vc at 1.8V), while there is minimal increase in current consumption, the amplifier can provide 1 to 2dBm more output power for LO or transmitter driver applications where high output power and linearity are often required.

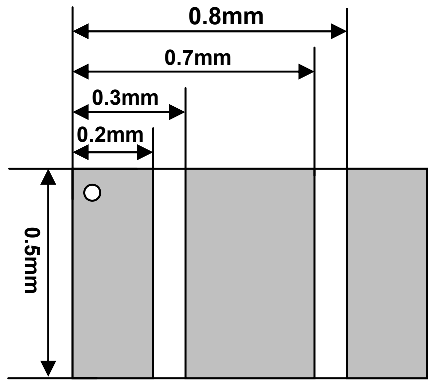
Refer the Absolute Maximum Ratings table for allowed DC and thermal conditions.

Outline Drawing

Top and Side View



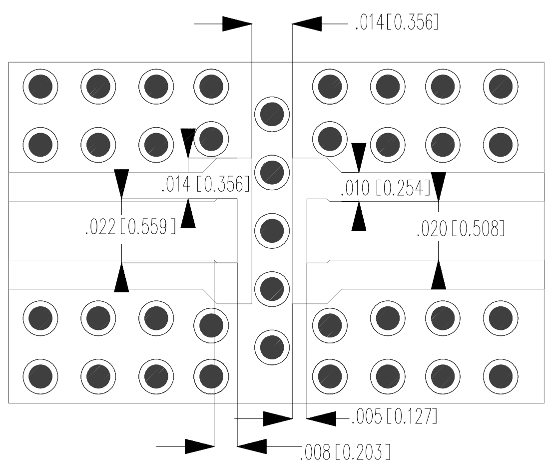
Bottom View



NOTES:

1. ● indicates pin 1
2. Dimensions are in millimeters
3. Pad Material is minimum 5.0 um thick Au

Suggested PCB Material and Land Pattern



NOTES:

1. 0.010” Rogers RO4350

Recommended SMT Attachment

The VMMK Packaged Devices are compatible with high volume surface mount PCB assembly processes.

<u>Manual Assembly for Prototypes</u>

1. Follow ESD precautions while handling packages.
2. Handling should be along the edges with tweezers or from topside if using a vacuum collet.
3. Recommended attachment is solder paste. Please see recommended solder reflow profile. Conductive epoxy is not recommended. Hand soldering is not recommended.
4. Apply solder paste using either a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance. ***Excessive solder will degrade RF performance.***
5. Follow solder paste and vendor’s recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temp to avoid damage due to thermal shock.
6. Packages have been qualified to withstand a peak temperature of 280°C for 15 sec. Verify that the profile will not expose device beyond these limits.
7. Clean off flux per vendor’s recommendations.
8. Clean the module with Acetone. Rinse with alcohol. Allow the module to dry before testing.

Note: These devices are ESD sensitive. The following precautions are strongly recommended. Ensure that an ESD approved carrier is used when die are transported from one destination to another. Personal grounding is to be worn at all times when handling these devices. For more detail, refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control

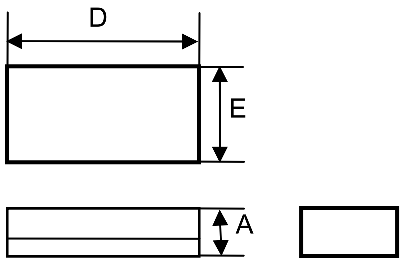
ESD Machine Model (Class A)

ESD Human Body Model (Class A)

Ordering Information

Part Number	Devices Per Container	Container
VMMK-2403-BLKG	100	Antistatic Bag
VMMK-2403-TR1G	5000	7" Reel

Package Dimension Outline



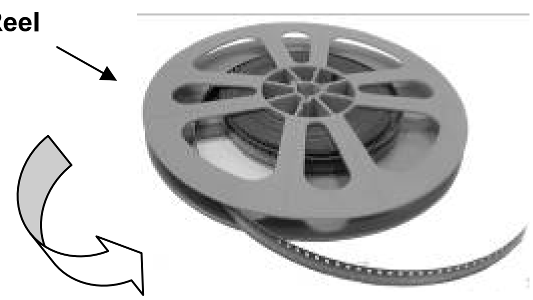
Dimensions

Symbol	Min (mm)	Max (mm)
E	0.500	0.566
D	1.004	1.066
A	0.235	0.265

Note:
All dimensions are in mm

Device Orientation

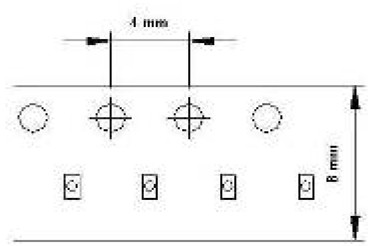
Reel



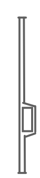
User Feed Direction

Carrier Tape

Top view



End view



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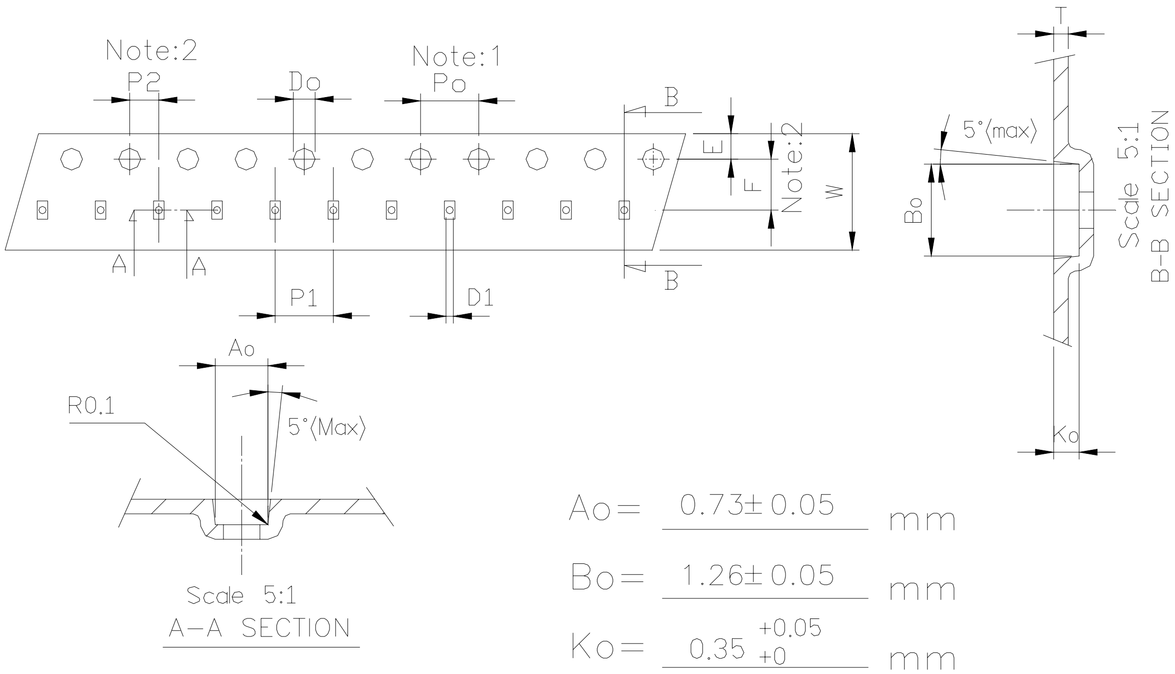

Unit: mm

Symbol	Spec.
K1	–
Po	4.0± 0.10
P1	4.0± 0.10
P2	2.0± 0.05
Do	1.55± 0.05
D1	0.5± 0.05
E	1.75± 0.10
F	3.50± 0.05
10Po	40.0± 0.10
W	8.0± 0.20
T	0.20± 0.02

Notice:

1. 10 Sprocket hole pitch cumulative tolerance is ±0.1mm
2. Pocket position relative to sprocket hole measured as true position of pocket not pocket hole.
3. Ao & Bo measured on a place 0.3mm above the bottom of the pocket to top surface of the carrier.
4. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Carrier camber shall be not than 1mm per 100mm through a length of 250mm.

For product information and a complete list of Avago contacts and distributors, please go to our Website:
www.avagotech.com/semiconductors
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Data subject to change.

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